APPLICATION NOTE

How to Measure Femtofarad Capacitance-Voltage at Transistor Contact Level

INTRODUCTION

Electrical Failure Analysis starts with finding the defective transistor on a semiconductor chip. Once the location is known, the next step is to use DC and AC measurements to characterize the transistor and find the root cause of the defect. DC techniques can help to determine the threshold voltage of the transistor or the gate leakage current [1]. Other important parameters are not as straightforward to measure, for example thickness of the gate oxide and the dopant concentration profile [2]. AC techniques, such as Capacitance-Voltage (CV) measurements, offer an effective way to measure these parameters.

In this application note, we show femtofarad-scale CV measurements at the gate of two MOSFET transistors. CV measurements help to examine various aspects of the gate oxide or to identify defects [3]. CV gives information about input and output capacitance of the transistor, gate oxide thickness, dopant density and flat-band voltage. It can also provide information on the gate oxide quality and interface charges [4].

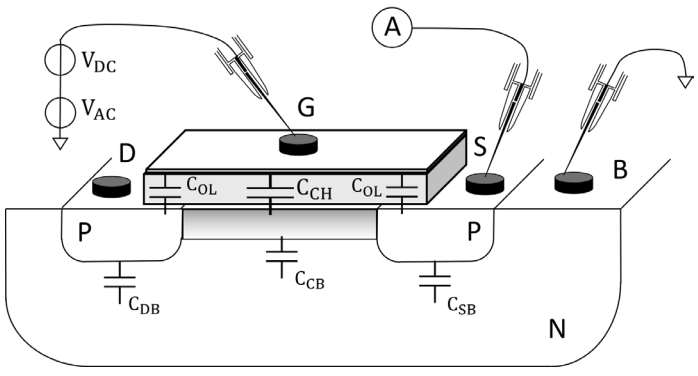

Figure 1. Schematic of a transistor cross-section with different capacitances involved in the CV measurements. In this case, the capacitance is measured between the gate (G) and the source (S), while the bulk (B) remains grounded.

CV measurements are usually done by connecting one probe to the gate of the transistor and the other probe to the bulk, source or drain (see Figure 1) [5]. Here, we apply DC bias with a superimposed AC signal to the gate and measure the current induced by the AC signal at the other terminal. The configuration shown in Figure 1 measures the capacitance between Gate and Source, while the Bulk is grounded to prevent any offset from the capacitances CCB, CSB and CDB. We calculate the impedance between the probes from the amplitude and phase shift of the current. We also show how to make sure that the measurement is not affected by noise, offsets, and parasitic inductances.

EXPERIMENTAL SETUP

Preparation of the experimental setup:

1. Deprocess the digital area of the device-under-test (DUT) to expose the contact level.

2. Mount the sample on a standard SEM stub and place it at the center of a Nanoprobing Platform (SM125) from Imina Technologies equipped with three miBot™ nanoprobers.

3. Load the platform in the SEM (here: Zeiss Sigma FE-SEM) and pump the system down.

4. Connect a semiconductor parameter analyzer (here: Keithley 4200A-SCS) equipped with a 4215-CVU (Capacitance Voltage Unit) to the nanoprobes using feedthrough connectors on one of the SEM flanges.

CV measurements on MOSFET gate transistors are challenging for a few reasons. First, the gates typically exhibit extremely low capacitances (fF). This range is an order of magnitude smaller than the intrinsic capacitance of the whole setup, so we need to measure the latter and compensate for it. Secondly, the measured AC current that is used to derive the capacitance is small, making the measurement sensitive to noise, offsets, leakage, and parasitic inductance. We must carefully implement precautions for low-current AC measurements: shield everything, minimize ground loops, put grounds in common, and separate voltage and current measurements. Lastly, the device under test is not a simple capacitance with two terminals: it comprises a complex set of metal lines and depletion regions. We need to understand the layout well in order to cancel or guard the right terminals to measure just the capacitance of interest and not several capacitances together.

To avoid noise, offsets, and other issues when measuring the AC current, we should be careful with the shields of the system and the wiring to the DUT. Figure 2 shows a schematic of the cabling from the DUT to the CVU. From Keithley's CVU, the HIGH terminal is split into HPOT and HCUR terminals. The LOW terminal is split into LPOT and LCUR. To minimize the effect of the parasitic capacitances and resistances of the cabling, we recommend bringing these HPOT/HCUR and LPOT/LCUR pairs together, as close as possible to the sample. We have done this by modifying the probe holders[1] to bring two independent signals together at the probe level (see Figure 2 - bottom panel). To minimize stray capacitances and ground loops, we suggest connecting the shields of these four wires inside the Nanoprobing platform[2] . Finally, to effectively cancel out the additional capacitance from the bulk, we have connected the bulk probe to the shields of the other signals (see the schematic on Figure 2 - top panel).

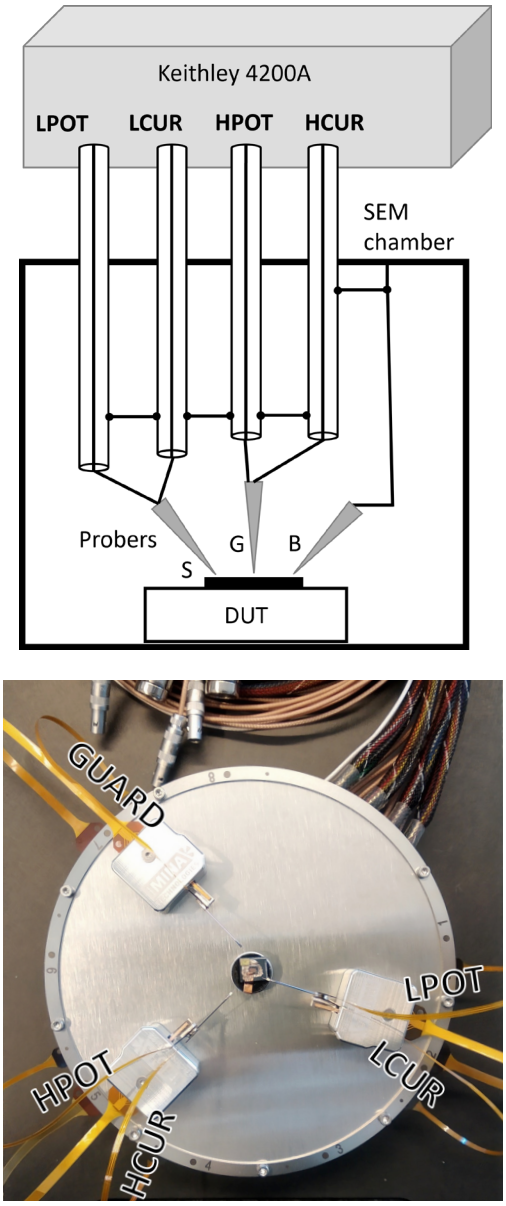

Figure 2. Schematic and picture of the CV measurement setup. The high and low signal pairs are brought together at the probe level. The shields of the lines are brought close inside the platform. The SEM chamber acts as a Faraday cage.

MEASUREMENTS

For the measurements, we have set the parameters of the CVU as follows:

- The sweeping DC bias from -2V to +2V
- AC voltage amplitude 100mV at 1MHz frequency.
- Acquisition time 3s per data point (enough time to average noise and keep a reasonable measurement time of a couple of minutes).

Before running the CV measurement on the transistor, we must correct for the parasitic capacitance of the setup. To do this, we have run a CV measurement with the circuit open (the probes not touching the transistor). The results are shown in Figure 3. The parasitic capacitance of the system is around 19fF, and we subtract this value from the data acquired on the transistor. The noise level at 50aF does not significantly affect the experiment.

1 LPOT/LCUR and HPOT/HCUR probes are modified to have two wires on each probe. Contact us if you need such modification for your system.
2 If you need to measure Capacitance-voltage, contact us and we will happily advise you how to do it

Now we can land the probes on the Gate, Source, and Bulk of the transistor and repeat the measurement. Figure 4 shows the compensated CV curve obtained for both PMOS and NMOS transistors and the SEM images of the probes landed on the contacts in each configuration.

The resulting curves show typical CV behavior of PMOS and NMOS transistors. In the charge accumulation regime, there is no conducting channel and the capacitance between the gate and the source is only that of the overlapping region (COL in Figure 1). At the opposite gate polarity, a channel connects the drain to the source. In this regime, the capacitance between gate and source is the sum of the capacitance from gate to channel (CCH) and both capacitances from overlapping regions (COL). The total capacitance seen from the gate of the transistor is measured at around 2.5fF. With these results, and if the gate area is known, we can calculate the oxide thickness, the doping profile, and the flat band voltage of the transistor. For our sample, the gate area is not known, and the error resulting from an estimation would be translated into large offsets of the calculated transistor parameters.

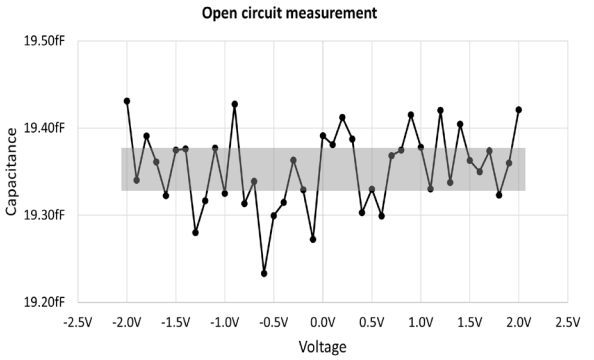

Figure 3. CV measurement run on the system in open circuit. It corresponds to the stray capacitance that needs to be compensated for. A noise of 50aF is measured (grey band on graph).

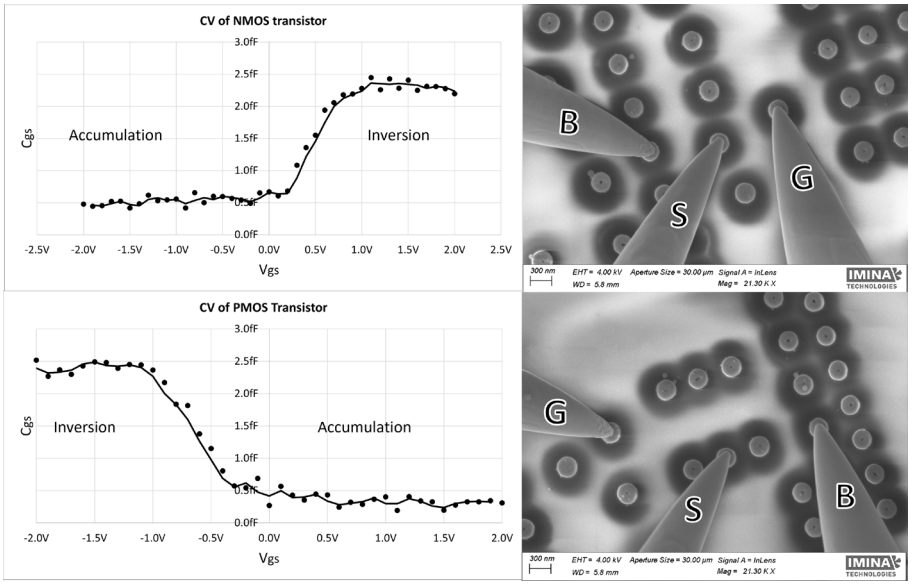

Figure 4. Compensated CV measurements and corresponding SEM images acquired on both a NMOS (top) and a PMOS (bottom) transistor. The shape of the curves reveals the accumulation and inversion regimes of the transistors.

CONCLUSION

We have shown how to measure fF-scale gate capacitance of a MOSFET exposed at the contact level. We could easily measure capacitances down to 2.5fF. We can measure such low capacitance thanks to: 1) Imina Technologies' probers being robust against noise; 2) Careful wiring of the Keithley CV Unit. The noise level amounts to as little as 50 aF, which means we can potentially measure sub-femtofarad capacitances with this setup. To measure larger capacitances, some of the modifications brought on the wiring would not be necessary, making the measurement setup and procedures simpler.

[1] "Analysis and Design of Mosfets", J.J. Liou, 1998

[2] "Active doping profile using Transmission Line Matrix method", A. Lounis, 2017

[3] "Applications of the pulsed current-voltage and capacitance-voltage techniques for high-resistive gates in MOSFETs", L. Lai, Microelectronics Reliability, 2016

[4] "MOS Transistors Characterization By Split C-V Method", S. Mileusnic, 2001 IEEE

[5] "C-V Testing for Components and Semiconductor Devices", Keithley Application Note Series

Imina Technologies SA
Route de Montheron 8b, 1053 Cugy (VD), Switzerland
www.imina.ch