APPLICATION NOTE

SEM-Based Nanoprobing for the Characterization of NMOS and PMOS Transistors on 22, 14 and 10 nm Semiconductor Devices

INTRODUCTION

With the continuous shrinkage of the component size of integrated circuits (IC), nanoprobing in scanning electron microscope (SEM) has become an increasingly used technique by IC design and failure analysis engineers to characterize the performance of microchips, as well as to locate and analyze the root cause of defects.

Whether a semiconductor lab is already equipped with underused SEM(s) or it is looking for a multipurpose microscope, versatile nanoprobing solutions that can easily be installed and removed from the chamber are becoming more and more desired. Also, with technology nodes equal to or smaller than 45 nm with high-κ materials into the gate stack, the positioning resolution of nanoprobers is no longer the only key factor of the nanoprobing system to be considered. As the acceleration voltage of the SEM and the working distance must be reduced, the maneuverability of nanoprobers offering a risk-free positioning of delicate probes, the stability of the tips in contact with the sample and the ability to efficiently conduct and collect measurements are also factors to consider.

The Nanoprobing Solutions from Imina Technologies include from 2 to 8 miBot™ nanoprobers and are available as “stage-mounted” or “load-lock” versions to adapt to nearly any SEM chamber. The system shielded cabling allows transistor characterizations, EBIC and EBAC/RCI analysis to be performed with excellent signal-to-noise ratio. The operator is assisted at each step of the nanoprobing workflow, from the nanoprobers placement around the device under test (DUT) and landing the probe tips in contact to setting up test recipes, running measurements and storing data.

In this note, we report an application of Imina Technologies’ Nanoprobing Solution to characterize NMOS and PMOS transistors of commercially available processors of 22 nm, 14 nm, and 10 nm technology nodes. Measurements on the 10 nm device are reported and discussed. The experiments were carried out at different sites in two different SEM with no permanent modifications required of the microiscopes.

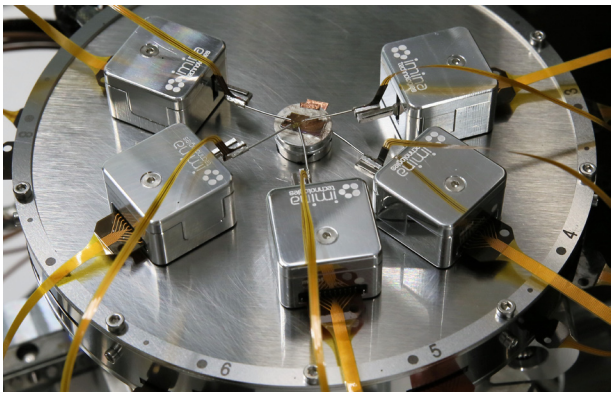

Figure 1. Five miBot™ nanoprobers around a semiconductor sample to test. The platform is mounted on the SEM motorized stage.

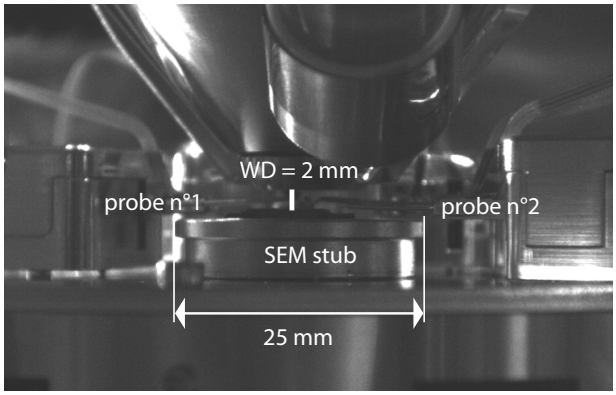

Figure 2. View from the SEM chamber scope on the miBot™ nanoprobers above the sample with a 2 mm working distance.

EXPERIMENTAL SETUP

For these experiments, the 8 miBot™ nanoprobing platform of Imina Technologies was used. It was installed at the beginning of the experiment on the motorized stage of the microscopes and the cables plugged into the electrical feedthrough connectors of the dedicated port. Depending on the sample, each miBot™ was equipped with a tungsten probe with a tip curvature radius (CR) of 20 nm or 10 nm and a tip bent at 40° (see Table 1). Electrical measurements were performed with a semiconductor parameter analyzer (Keithley 4200A-SCS) equipped with four 4210-SMU modules. It was operated from Imina Technologies Precisio™ nanoprobing software.

SYSTEM PREPARATION

The samples used for these experiments were delayered down to metal 1 so that single transistors of the SRAM cells located on the cache area of the processors could be independently electrically characterized. The samples were mounted with silver glue on standard 12.7 mm diameter SEM stubs with 2.5 mm height extender. The assemblies were placed in the electrically grounded stub holder at the center of the nanoprobing platform.

When the sample was in place, the position of the miBot™ nanoprobers were then quickly adjusted around to optimize the orientation of probes and place the probe tips close to each other near the region of interest (ROI). It was done by sliding the miBot™ on the platform by hand and by means of the high-speed mode of their piezoelectric actuators. This step did not require to open the chamber more than 10 to 20 minutes. After high vacuum was established again in the chamber, a typical 10 to 40 minutes cycle of in situ Plasma cleaning was run to remove inevitable traces of hydrocarbon contamination and reach thermal stabilization.

During this time, measurement test recipes were configured from Precisio™ nanoprobing software to remotely control the parameter analyzer. The actual wiring between the measurement channels (SMUs) and the miBot™ probes was configured from the graphical user interface. Predefined test recipes for NMOS and PMOS transistor characterization were selected and their parameters such as the current compliance, current and voltage range, and number of test points were tuned based on the theoretical properties of the DUT (Figure 3).

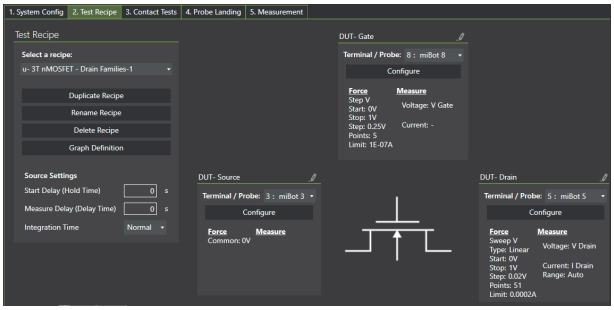

Figure 3. Electrical test recipes configuration view of Precisio™ software that will be run on the remotely controlled semiconductor parameter analyzer.

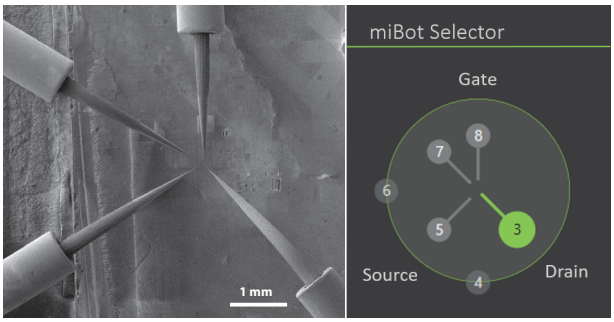

Figure 4. (left) Four nanoprobes positioned above a delayered area of a 14 nm Intel processor. (right) The prober selector in Precisio™ software.

Sample	Technology Node	Probe Tips	SEM	Working Distance [mm]	Acceleration Voltage [kV]
Intel Core i3 4160	22 nm	CR = 20 nm, bend = 40°	Zeiss Gemini 300	2.00	1.0
Intel Skylake G4400	14 nm	CR = 10nm, bend = 40°	Tescan S8000 (BrightBeam column)	2.19	0.5
Samsung Exynos 8895	10 nm			2.17	

Table 1. Details of the equipment used to test the semiconductor samples.

After the cleaning process was ended, the microscope parameters were set to optimize image quality while preserving the integrity of the DUT. Typically, for technology nodes equal to or smaller than 45 nm, the acceleration voltage should not exceed 500 V. At low acceleration voltage, working distances (WD) must be short to resolve single transistor contact, typically below 2.5 mm in our cases. Only for the 22 nm sample, the acceleration voltage was eventually set to 1 kV to improve image quality on the Zeiss Gemini 300.

TRANSISTORS PROBING

Prior knowledge of the position of the test area on each circuit and the orientation of the sample in the SEM was helpful to efficiently find the location to probe at low magnification. Once the corresponding coordinates of the SEM motorized stage were noted, the sample was moved horizontally a few hundred nanometers away. The next step consisted in bringing all probe tips in the field of view in contact with the sample surface (Figure 4). To maintain good imaging resolution at higher magnification, the SEM stage was moved up to reduce the WD as the probes were lowered. After all probe tips touched the surface, they were lifted and horizontally moved above the transistor to characterize.

The probes tips were sequentially lowered down in contact with each transistor node. Switching from one prober to another and adjusting their speed and positioning step size was intuitively done using the control pad. Once all probes had touched down, the beam was deflected away from the test area to avoid affecting electrical measurements. Precisio™ contact test module was then used to quickly check the quality of electrical contacts by repeating fast measurements. When required, probes position was slightly adjusted until measured curves become characteristic of the DUT (Figure 5).

MEASUREMENTS

Before starting the characterization of transistors, leakage current of each channel was measured when probes were not in contact with the DUT. It was lower than 200 fA on all channels.

The transistors were characterized by measuring the Drain current I_D when sweeping Drain-Source voltage V_{DS} at different Gate-Source voltages V_{GS} ($I_D=f(V_{DS})$) and when sweeping Gate-Source voltage V_{GS} for different Drain-Source voltages V_{DS} ($I_D=f(V_{GS})$). Source current I_S and Gate current I_G were also measured. Figures 6 and 7 show respectively the characteristics of NMOS and PMOS transistors of the 10 nm device. The test recipes for this device were configured with a current compliance on I_D and I_S set to 100 mA. The Drain and Gate voltage sweeps were made in 31 steps of 0.02 V. The Drain and Gate voltage bias were made in 4 steps of 0.20 V.

The measurements were run directly from Precisio™ software. Measurements are displayed with a graph and a table of values. Both are stored on the computer along with the parameters of the test recipe for post-processing and reporting.

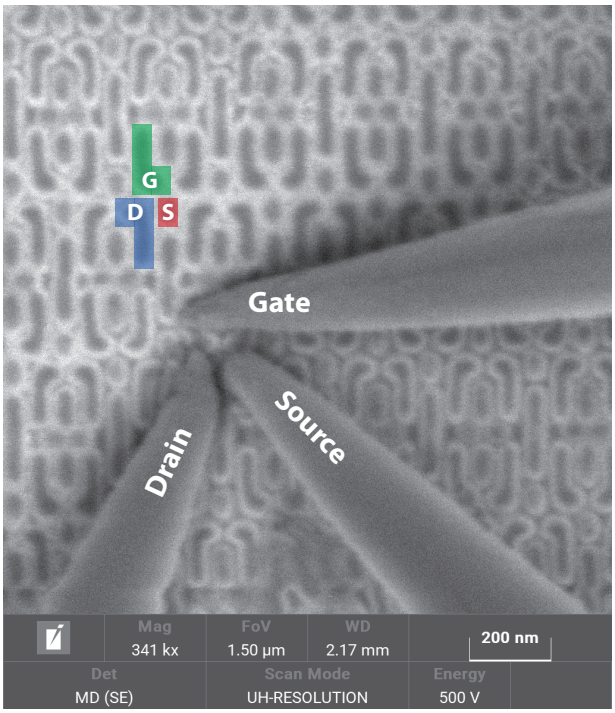

Figure 5. Three nanoprobes in contact with the Drain, Source and Gate of a PMOS transistor at Metal 1 (Samsung Exynos 8895, 10 nm technology node).

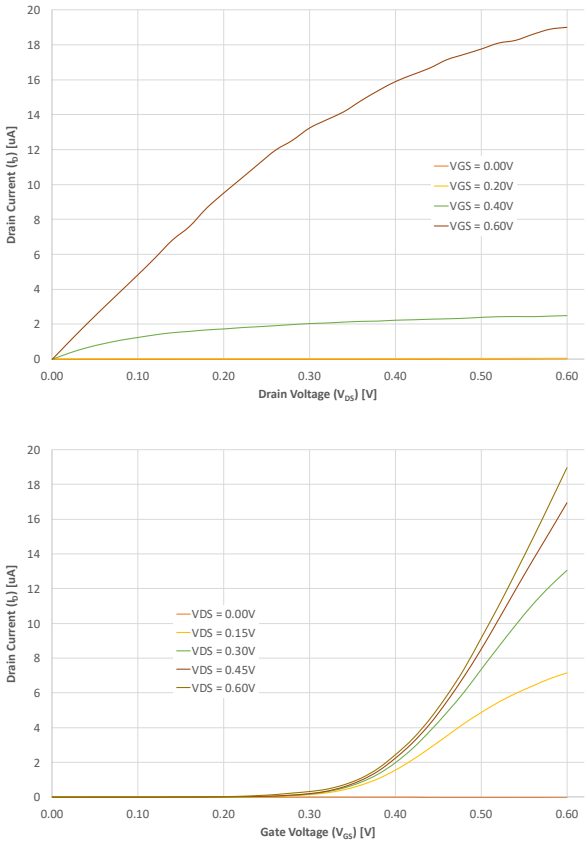

Figure 6. NMOS transistor characteristics (10 nm technology). (Top) Drain current vs Drain-Source voltage sweep. (Bottom) Drain current vs Gate-Source voltage sweep.

RESULTS AND DISCUSSION

Plotted curves are consistent and smooth. The difference between Drain and Source currents was calculated over the measured range and the normalized standard deviation is smaller than 0.2%. This low value proves the excellent stability of the contact resistance during measurement. Also, measurement noise and resolution are very good. For instance, on NMOS transistor with V_{GS} = 0V (transistor OFF), Drain current I_D was lower than 10 pA with V_{DS} = 0V and lower than 5 nA with V_{DS} = 0.6V.

At such small dimensions, thermal drift is inevitable. This can even result in a loss of electrical contact of the probe tips with the transistor nodes. As a matter of comparison, on the 22 nm sample, I-V sweeps were repeated every 10 minutes for over an hour without the probes to lose contact. On the 10 nm sample, the probe tip that was first landed lost electrical contact about 10 to 15 minutes later. This amounts to a drift of less than 1 nanometer per minute. This limited sensitivity to thermal drift of Imina Technologies nanoprobing system is the combined benefit of the compact and monolithic design of the miBot™ nanoprobers, the short distance between the probe tip and the robot body and the fact that the sample and the nanoprobers are mounted on the same support.

CONCLUSIONS

Several nanoprobing experiments were conducted to characterize NMOS and PMOS transistors of commercially available processors with 22 nm, 14 nm, and 10 nm semiconductor technology nodes. The results demonstrated the capability of Imina Technologies' Nanoprobing Solutions to perform reliable measurements in different scanning electron microscopes. We showed that the unique motion technology of the miBot™ nanoprobers helped to position probe tips with ease on the device under test. Their compact design proved to be advantageous to maintain stable electrical contacts for over 10 minutes to more than an hour.

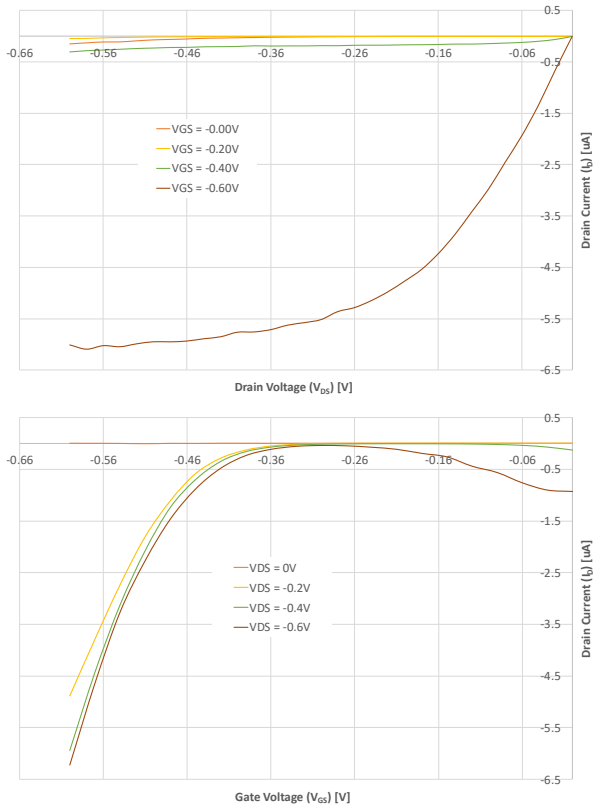

Figure 7. PMOS transistor characteristics (10 nm technology). (Top) Drain current vs Drain-Source voltage sweep. (Bottom) Drain current vs Gate-Source voltage sweep.

Imina Technologies SA
Route de Montheron 8b, 1053 Cugy (VD), Switzerland
www.imina.ch