

## APPLICATION NOTE

# Circuit editing and failure analysis performed at FIB tilt angle position combining GIS, EBAC and nanoprobe techniques

## INTRODUCTION

In the field of semiconductors failure analysis (FA), the selection of the investigation technique to be used is heavily dependent on the required time per analysis and the accuracy of the results obtained [1]. A recent trend to optimize these two variables is to combine the use of different tools and techniques to get more accurate data at a faster rate. As an example, passive voltage contrast (PVC) alone was used to determine opens and shorts in a circuit, which is now being replaced by a combination of nanoprobe and Electron Beam Absorbed Current (EBAC) measurements [2]. In this technique, two probes are landed, one on a local signal line and one at the ground of the sample. These probes collect the charges generated by the electron beam and absorbed by the sample. If there is a low resistive path between the area where the beam is injecting charges and the signal probe, this area will appear bright on the image. However, if there is no direct path to the signal probe, the charges will sink to the ground probe, causing the corresponding area appearing dark on the image. This allows the user to determine with high accuracy which lines of a circuit are connected to each other, making it an indispensable tool to detect shorts and opens on otherwise difficult to analyze circuit [3]. Another important tool in FA investigations is the Focused Ion Beam (FIB), as it has become the standard tool to artificially create opens and shorts in a circuit as well as to prepare Transmission Electron Microscope (TEM) lamellas [4]. However, most FIB uses are done under a stage tilt angle of 50-54°, which corresponds to the position where the ions are hitting the sample surface perpendicularly. Therefore, if a nanoprobe system needs to be used in conjunction with a FIB, the probing system must comply with the tilting requirements of the stage.

Moreover, a workflow combining nanoprobe, EBAC and FIB will undeniably benefit the semiconductor FA community as it allows greater accuracy and flexibility compared to applying each of these techniques independently. However, the turn-around time allocated for analysis must remain as short as possible. One way to achieve this is to align the different tools once and perform all the required measurements within that alignment. This means bringing the sample under 5mm working distance (WD) at a tilt of 54° and using both the nanoprobe system and EBAC in this configuration. The nanoprobe system must therefore be able to move and land probes while the microscope stage is at the FIB tilt position. In this article, we developed a workflow capable

### In collaboration with:

Fraunhofer IMWS  
Halle, Germany  
[www.cam.fraunhofer.de](http://www.cam.fraunhofer.de)



### Imina Technologies products in use:

- miBot™ BT-14 nanoprobe
- Nanoprobe SEM Platform kit

### Published in EDFA magazine:

[www.asminternational.org/web/edfas/news/edfa](http://www.asminternational.org/web/edfas/news/edfa)

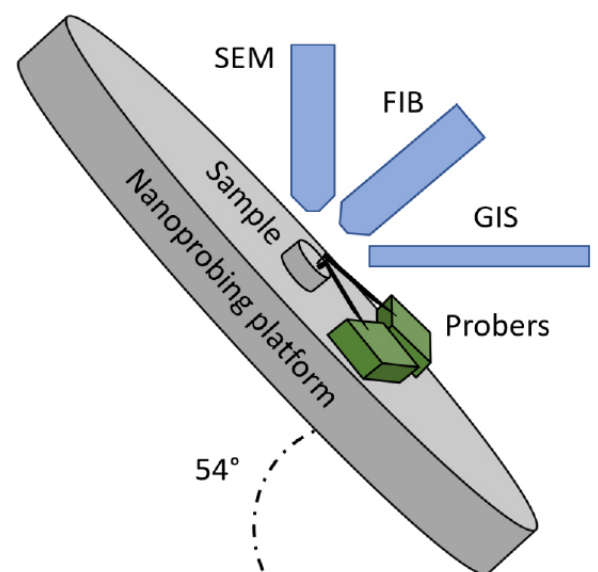


Figure 1. Schematic of the nanoprobe platform tilted to FIB position. It must be raised such that the sample is at the coincidence point of the electron and the focused ion beams.

of such performances and applied it to two typical FA and circuit editing use cases. The first one is a controlled GIS-assisted (Gas Injection System) FIB induced deposition of a pull-up resistor between two networks. The second one is an investigation of the localization of a short between two metal layers using EBAC and FIB metal line cutting.

## EQUIPMENT

A FIB-SEM microscope equipped with a gas injection system from Carl Zeiss AG was used for this experiment. An 8-prober nanoprobe platform from Imina Technologies SA was installed on the motorized sample stage and electrically connected through a port of the chamber with a custom flange. Two miBots™ (probers) were mounted on one side of the platform to allow for easy tilting in the opposite direction of their placement. These probers allow to position probes in XYZ with nanometer resolution over centimeters range. They move freely over the platform and stick to it with a small magnet enclosed under their body. These magnets are strong enough to allow the probers to climb the 54° slope imposed by the FIB tilt position but are located far enough from the beams to not disturb them in any ways. The needles were mounted on the miBots™ such that their roof is on the same plane as the needles when the prober arm is horizontal (Figure 2).

This configuration allows imaging at short WD (5mm in this case, but as low as 2mm for other applications) when tilted by avoiding collisions between the probing system and the pole piece of the microscope. Outside of the microscope chamber, a semiconductor parametric analyzer from Tektronix Inc. (Keithley 4200) and an EBIC/EBAC imaging system from Point Electronic GmbH were electrically connected to the probes through the flange feedthrough connectors, respectively for case studies 1 and 2.

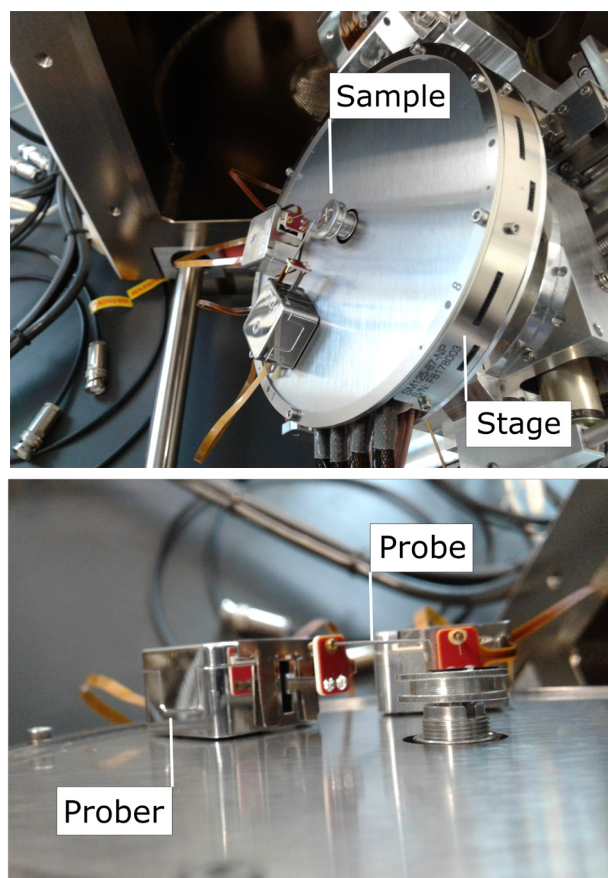


Figure 2. miBot mounted in the Zeiss Auriga. Left: tilted at 54° with the two probers at the lowest position to avoid collision. Right: with the probes in the same plane as the prober's roof to allow short working distances.

## CASE STUDY 1: Circuit editing - Pull-up resistor deposition

In some cases of circuit editing, a reference voltage may be needed at a specific node of an Application-Specific Integrated Circuit (ASIC) sensor. For this, a pull-up resistor of 1 kOhm can be deposited in between two distinct networks.

The deposition process consists of injecting with the GIS a precursor gas that is decomposed at the surface by an external energy source. Either the electron beam or the FIB can be used for that purpose, although the FIB provides faster deposition rates. The process described in this case study is divided into three main steps: 1) deposition of the resistor terminal pads connected to the two networks; 2) deposition of a baseline resistor using the electron beam; 3) deposition of the resistor with the FIB with live monitoring of its value.

To get access to the networks, the FIB was first used to remove the passivation layer at the locations where the resistor terminals will be placed. Two micron-sized pads were then deposited at these locations to ensure good contact with both networks and provide convenient access to the resistor terminals while it is being deposited.

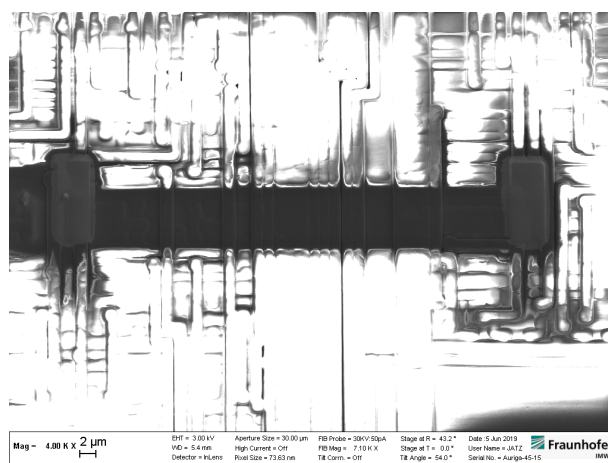


Figure 3. Platinum layer deposited between the two pads using the electron beam. It serves both as a protective layer from undesired FIB milling and as a baseline resistor for the in-situ resistance monitoring.

A thin layer of Platinum was deposited between the two freshly created pads using the electron beam (Figure 3). This layer serves both as a protective layer from possible unwanted milling from the FIB and as a baseline resistor to monitor the resistance during FIB-induced deposition. It is worth noting that ten minutes were required to deposit this first layer of approximately 60kOhm resistor using the e-beam, which justifies the use of the FIB to deposit the 1kOhm as its deposition rate is much higher. Once this baseline resistor was deposited, the stage with the probing system were tilted to FIB position at 54°, alongside the GIS nozzle, as shown on Figure 4.

At this tilt angle, horizontal alignment and landing of the probes in contact with the terminal pads was rapidly achieved with the nanometric motion resolution of the miBots™. Prior to the deposition, the baseline resistor was measured again, to check the good electrical connection between the probes. Platinum deposition was then initiated at the same time as a 1V bias was applied with the source-meter unit between the probes. The current flowing between them was continuously monitored during the deposition as depicted in Figure 5.

The FIB and gas insertion were stopped once the desired value of 1mA was reached. The obtained resistance was then measured at exactly 1.00 kOhm, which shows the advantage of being able to measure the resistance while it is being deposited.

As the deposition did not take place on an entirely flat substrate (Figure 6), the effect of the sample topography impacts the speed at which the resistance changes over time. In fact, since it takes more time to deposit Platinum on the vertical sides of the metal tracks, these areas act like bottle necks for the current, increasing the overall resistance. As the layer gets thicker, the topographic profile smoothens and this effect dampens, leading to a higher resistance change rate. This results in slope changes of the graph curve in Figure 5.

The resistance deposition process described in this case study, from the baseline resistor deposition to the final resistor deposition took approximately 45 minutes. This fast pace was possible as all the steps were made in a row without having to tilt the sample back and forth between 0° and 54°. Live current monitoring during the resistor deposition also clearly provides a gain in accuracy of the resistance value which would be impossible to match if the probes could only be landed at 0° tilt.

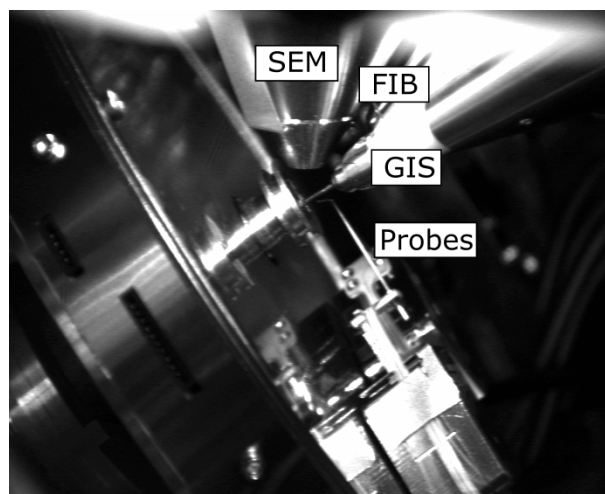


Figure 4. Chamber scope view of the platform in operating conditions at FIB tilt position with the GIS nozzle inserted. The sample is at the coincidence point of the two beams.

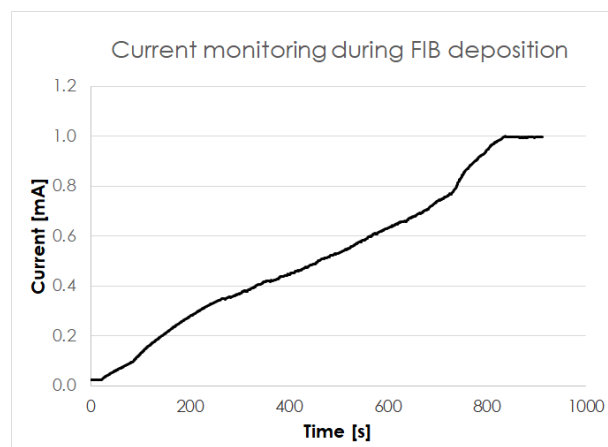


Figure 5. Live monitoring of the current in between the two probes while the resistor is being deposited. A voltage difference of 1V is applied to the probes.

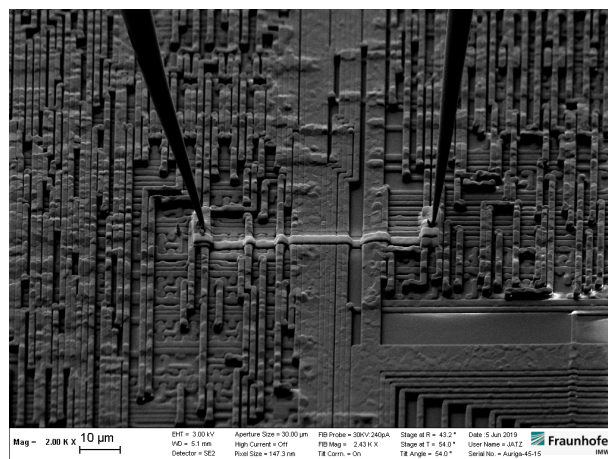


Figure 6. SEM image under 54° stage tilt of the resistor obtained at the end of the FIB induced deposition. The probes are landed on the resistor terminals to measure its value.



Localizing shorts in integrated circuits is part of the daily routine of many semiconductor failure analysts as it is the first step before further defect investigation. EBAC imaging for highlighting interconnected networks, and FIB for cutting lines, are premium tools for shorts localization. Figure 7 illustrates the principles of that process. The “green” metal line has an unwanted connection with the “red” metal line. A nanoprobe in contact with the first line is used to produce EBAC images of the interconnected lines. To identify if the short is located at a crossing point, the red line is FIB cut close to where it crosses the green line. After the cut, if the inferior fraction of the red line overlapping the green line does not appear in the EBAC image anymore, there is no short between the lines at this location (Result 2). On the contrary, if this fraction remains visible, it means the short is located at this crossing point (Result 1).

In this case study, we describe the defect localization of a short on an ASIC from the automotive industry which was identified to behave abnormally. After electrical characterization at the bond pad level, it appeared that one of the signals does not switch correctly and instead keeps a constant low. The chip was decapsulated and mounted on a SEM stub using conductive glue. As in the first case study, after identifying the corresponding network on the chip, an opening in the passivation layer was made using the FIB. A contact pad was deposited to give access to the network via nanoprobing.

To produce the EBAC images, the probe connected to the input high of the EBAC amplifier was first landed on the contact pad, while the other probe connected to the input low of the amplifier was put in contact with the local ground of the circuit. As a matter of comparison, Figure 8 shows on the left, an image of a functioning device with only one highlighted metal line and, on the right, an image of the failing device with many highlighted lines. This means that not only the suspected network (Signal A) is lighted up, but also another network at a superior metal level (Signal B), clearly suggesting that the two are shorted. The networks cross each other at four different locations where the short could be located, hence all four sites were investigated.

The short investigation procedure was followed. The microscope stage was tilted to FIB position at 54° and the probes were aligned and landed on their respective contacts (ground pad and Signal A). For each crossing point, rapid EBAC images were taken at intervals during the FIB milling of Signal B and used to determine when the track is successfully cut. High quality EBAC images, taken at the FIB tilt position before and after each cut, are reported in Figure 9. At crossing points #1 and #2, Signal B did not turn dark after the FIB cuts, indicating that there is no short at these locations. After the cut at crossing point #3, Signal B did turn dark except for its part directly located near this crossing point, clearly highlighting the behaviour of a short at this crossing point. This conclusion is also confirmed by the EBAC image made after the third cut at crossing point #4: only Signal A is lighted up as the short was isolated. At this point, a semiconductor FA engineer has high confidence that the defect in his faulty device was localized with precision. He can proceed with further investigations to characterize the source of this defect, for instance by making cross sections in the area of the crossing point or by preparing TEM lamella.

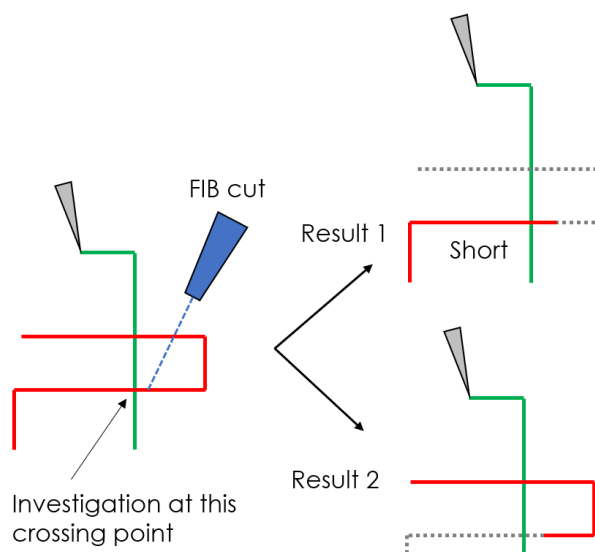


Figure 7. Schematic of the procedure used to determine if a short is located at a specific crossing point. If the crossing point can still be seen on the EBAC image after the cut, the short location has been identified.

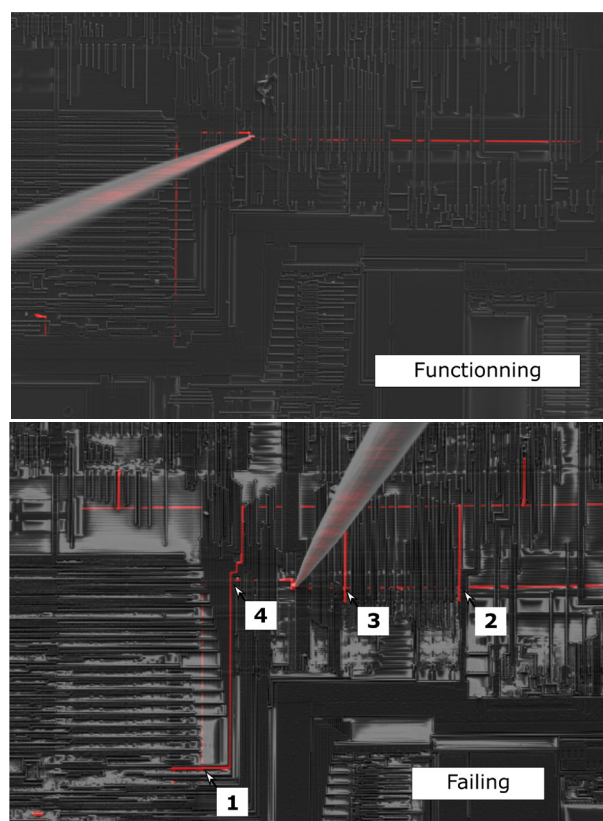


Figure 8. EBAC pictures of the suspected network taken on both a functioning device (left) and the failing device (right). An additional network appears on the failing device image. The four networks crossing points are indicated.

In this article, two use cases of common semiconductor failure analyses are presented, namely circuit editing and short localization. They describe a workflow that combines FIB, GIS, and nanoprobe techniques. The entire procedures are performed at the FIB tilt position (54°), avoiding the need to bring the motorized microscope stage back to horizontal position for nanoprobe after each FIB process. This provides several advantages, starting with the length of investigations which is greatly reduced. Avoiding unnecessary movements also has the positive side effect that it reduces the risk of collisions inside the microscope chamber. Finally, the ability of live monitoring the current flow with nanoprobe in the device under test during a FIB process, either with a source-meter unit or an EBAC imaging system, allowed us to reach higher accuracy in terms of fault localization and performance of circuit modification.

#### References

[1] J. Chin, V. Narang, X. Zhao, *Fault isolation in semiconductor product, process, physical and package failure analysis: Importance and overview*, *Microelectronics Reliability*, 2011, Volume 51, pp. 9-11

[2] L. Chang, K. Wang and S. Wang, « *The investigation of Active VC and EBAC Analysis Utilization on Test Structure* », *IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2015, pp. 205-208

[3] M. Simon-Najasek, « *Defect localization using SEM based current imaging* », *International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2018, Tutorial-B4

[4] Verkleij, D., « *The use of the Focused Ion Beam in failure analysis* », *Microelectronics Reliability*, 1998, Volume 38, pp. 6-8

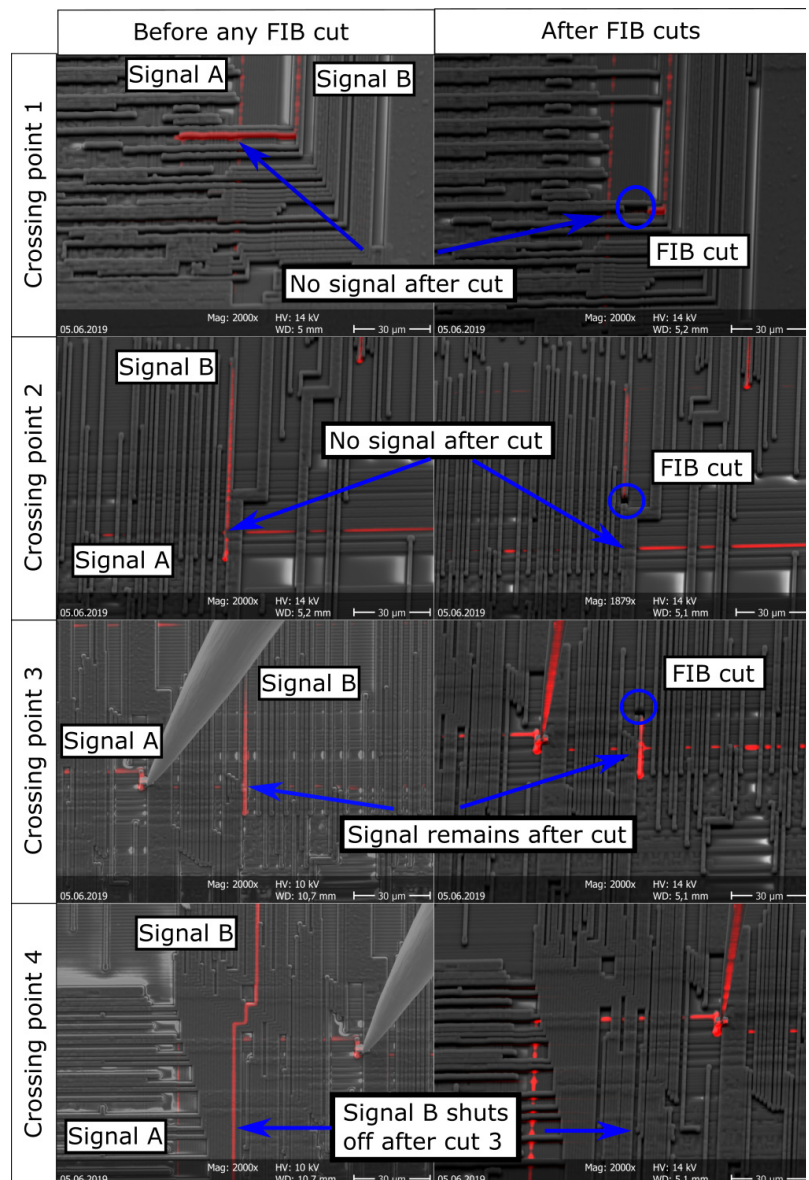


Figure 9. EBAC images of crossing points before (left) and after the FIB cut (right). At crossing points #1 and #2, the FIB cut shuts off the part of the faulty network (Signal B) crossing with the valid network (Signal A), indicating there is no short at these two locations. At crossing point #3, the FIB cut does not shut off the part of Signal B indicating the presence of a short. The last row confirms the short is localized at crossing point #3 as Signal B has turned dark.