APPLICATION NOTE

Transistor characterization of a 5nm SRAM die

INTRODUCTION

The components of integrated circuits (IC) are getting smaller and smaller. To keep up with this trend, IC design engineers increasingly rely on in-situ scanning electron microscope (SEM) nanoprobing. It serves to characterize the performance of microchips and to find faulty components, helping to optimize the IC design.

Electrical probing of nodes under 45 nm, with high-κ materials in the gate stack is challenging and time consuming. One has to operate SEM under low acceleration voltage and at short working distance. The position of the probes must be precisely controlled, and it is crucial to maintain a stable electrical contact between the probes' tips and the sample. Such time- and effort-intensive measurements depend on optimized workflow in order to reduce the time-to-data and be overall feasible. In this application note, we characterize NMOS and PMOS transistors of a 5 nm technology node chip to show the capabilities and the workflow of Imina Technologies' Nanoprobing Solution.

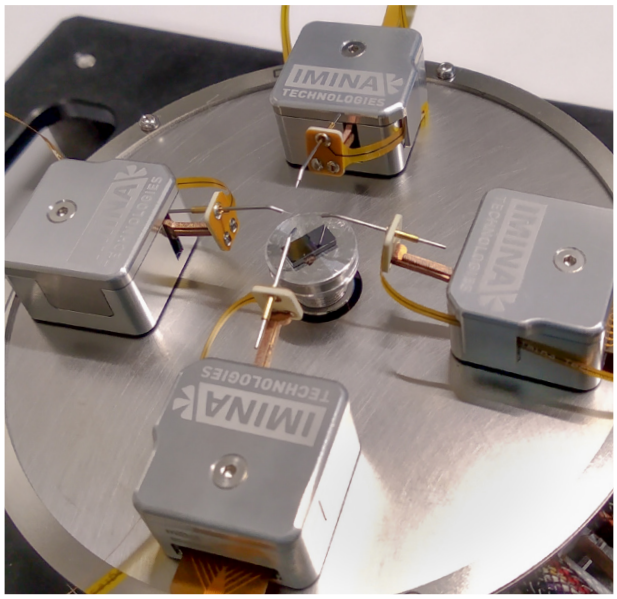

Figure 1. Four miBot™ nanoprobers around a semiconductor sample to test. The platform is mounted on the SEM motorized stage.

EXPERIMENTAL SETUP

TESCAN CLARA SEM is equipped with the following electrical probing setup:

- Imina Technologies' nanoprobing platform with four miBots™
- Tungsten probes, radius of the tip curvature 10 nm, the tip bent at 40° for each miBot™
- Semiconductor parameter analyzer Keithley 4200A-SCS equipped with four 4210-SMU modules operated from Imina Technologies Precisio™ software (Nanoprobing Workflow edition 2022).

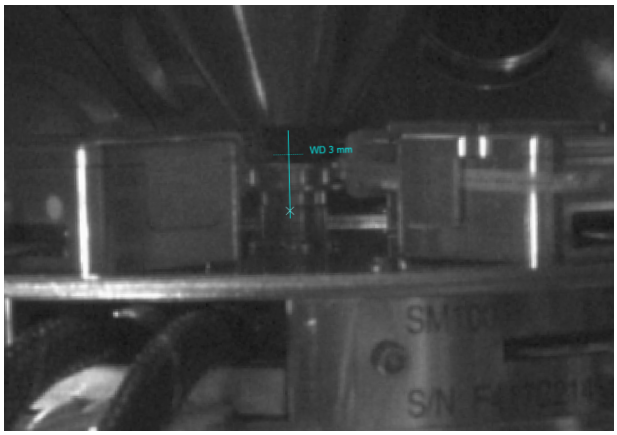

Figure 2. View from the SEM chamber scope on the miBot™ nanoprobers above the sample with a 2.8 mm working distance.

SAMPLE PREPARATION AND CHARACTERIZATION

The sample needs to be delayered down to Metal 1 for independent access to single transistors of the SRAM cells. The sample is first mechanically polished down to metal M5 layer. Gas-assisted Xe Plasma FIB delayering is used to remove all layers down to M1 layer through series of small windows of 25 µm × 25 µm. For that, the sample is mounted on a standard SEM stub and processed by TESCAN using

5 keV focused ion beam (FIB) with current of 1 nA. Finally, a cleaning process at FIB 3 keV, 1 nA, for a few tens of seconds is applied to minimize ion amorphization on the exposed layers.

Plasma cleaning is crucial to prevent hydrocarbon contamination on the sample and the probers' tips. For this step, we used a GV10x Downstream Asher from IBSS Group. The stub with the delayered sample is then placed on the electrically active[1] stub holder. Once the sample and the nanoprobing setup are inside the SEM and the chamber is pumped, a 35W plasma is applied for 2 minutes. Such plasma exposure is sufficient to prevent contamination during the experiment, while not oxidizing the sample or probes.

TRANSISTOR CHARACTERIZATION

In this experiment, the acceleration voltage of the SEM is set at 500 V and the working distance at 2.88 mm to resolve single transistor contacts. To efficiently find the region of interest at low magnification, it is very helpful to have prior knowledge of the test area position on each circuit and of the sample orientation inside the SEM. When at the right spot, the probe tips are sequentially lowered until they are in contact with transistor terminals. Here, the control pad is very convenient for switching from one prober to another and for adjusting their speed and step size.

To run the measurements, one can configure or choose predefined NMOS and PMOS test recipes for Precisio™ software to remotely control the parameter analyzer. The parameters such as the current compliance, current and voltage range, and number of test points are chosen based on the expected properties of the device under test (DUT) as shown in Fig 3.

Precisio™ contact test module helps to monitor the quality of electrical contacts. The probes' position should be adjusted until the measured curves become characteristic of the DUT. After this step, the measurement sequence can be launched. V_G-I_D and V_D-I_D curves for NMOS and PMOS are recorded using the following parameters:

V_G-I_D: Sweep V_{DS} (I_D=f(V_{DS})) in 0.033 V steps from 0 to 1V (respectively -1V) at different values of V_{GS}.

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All the measurements are run directly from Precisio™ software. The results are displayed as they are acquired with a plot and a table of values. Both are stored in the Precisio™ database along with the parameters of the test recipe for post-processing and reporting.

Notations

I_D – Drain current

V_{DS} – Drain-Source voltage

V_{GS} – Gate-Source voltage

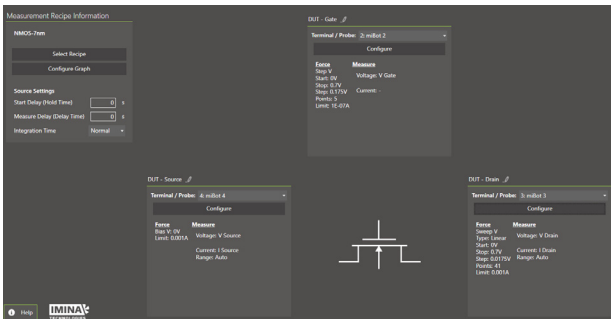

Figure 3. Configuration of electrical test recipes in Precisio™ software for the remotely controlled semiconductor parameter analyzer

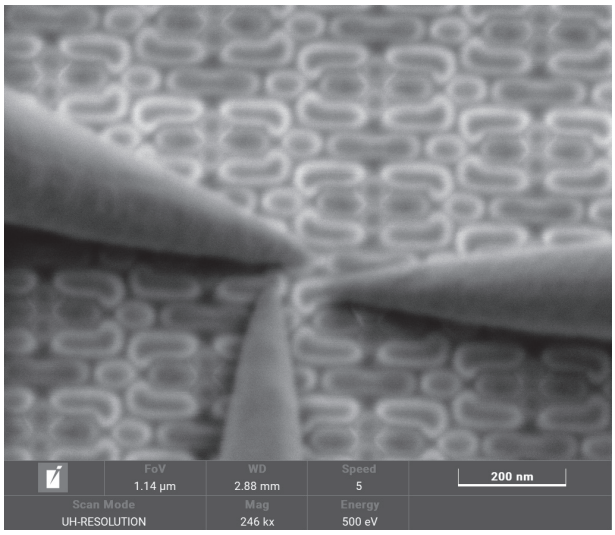

Figure 4. PMOS transistor

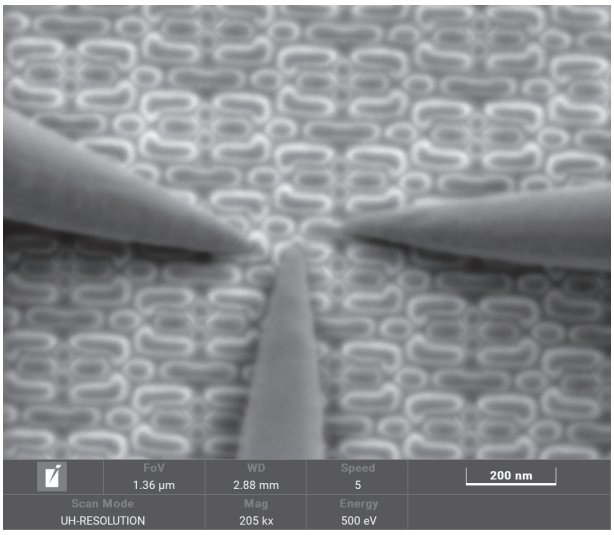

Figure 5. NMOS transistor

1 can be grounded or biased

RESULTS AND DISCUSSION

Plotted curves are consistent and smooth and show typical behavior for NMOS and PMOS transistors.

Noise and measurement resolution: on NMOS transistor at V_{GS}= 0V (transistor OFF), Drain current I_D < 0.2 pA at V_{DS}= 0V and I_D < 0.3 nA at V_{DS}= 0.7V. The current of less than a picoampere measured at 0V highlights low noise and leakages of the system. Such low noise allows to accurately measure the transistor $I_{D\text{-}off}$ of 0.3nA .

CONCLUSION

We characterized NMOS and PMOS transistors on 5 nm semiconductor technology nodes using Imina Technologies' Nanoprobing Solution inside the TESCAN Clara SEM. Such small nodes are challenging to image because SEM should operate under low acceleration voltage and at short working distance. Electrical characterization is also extremely demanding because the probes must be precisely positioned, a stable electrical contact between the probes' tips and the sample has to be maintained during the whole experiment. Our results demonstrate the capability of Imina Technologies' Nanoprobing Solution to perform reliable measurements on such small nodes. Our Nanoprobing Solution also offers tools to optimize the workflow, significantly reducing time-to-data.

miBot™ nanoprobers' compact design proves to be advantageous to maintain stable electrical contacts over time. The Nanoprobing Solution from Imina Technologies includes two to eight miBot™ nanoprobers and comes in a "stagemounted" or "load-lock" version to adapt to nearly any SEM chamber. The system's shielded cabling allows transistor characterizations, as well as EBIC and EBAC/RCI analysis with excellent signal-to-noise ratio. The Sample Positioning XYZ Sub-Stage enables lateral movements from one sample area to another without having to move the probers one by one. The operator is assisted at each step of the nanoprobing workflow: the nanoprobers placement around the DUT, landing the probe tips in contact, setting up test recipes, running measurements and storing data.

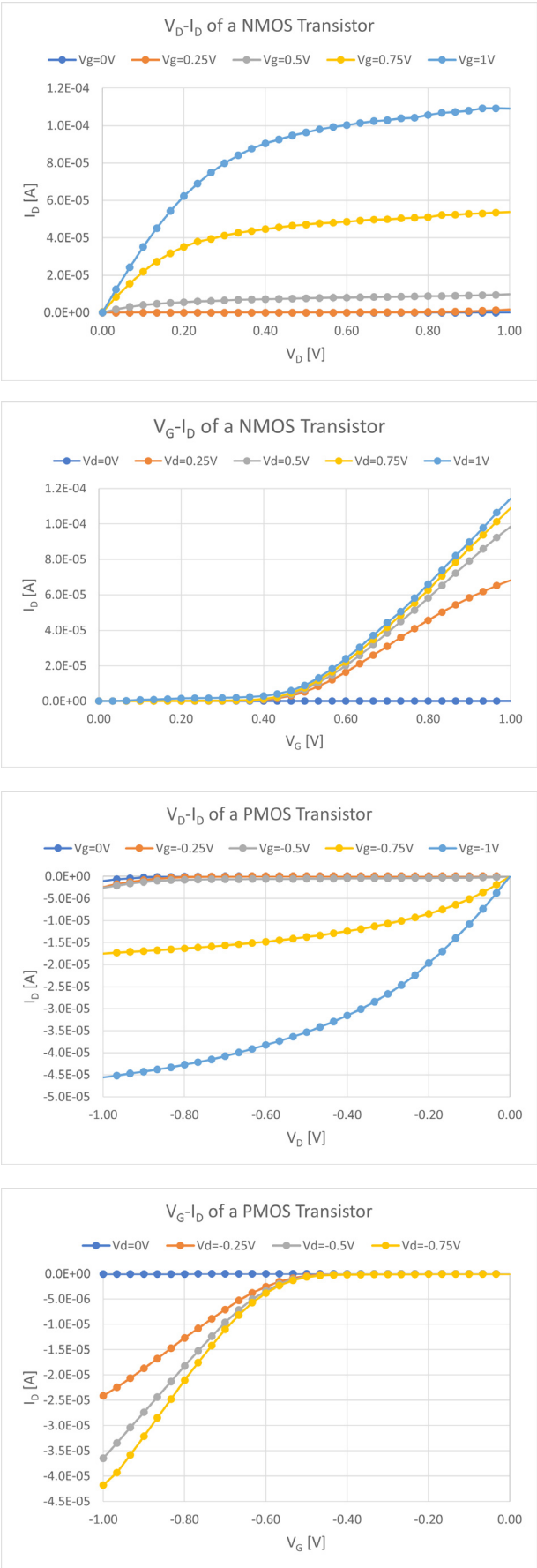

Figure 6. "Vd-Id and Vg-Id curves of NMOS and PMOS transistors from a 5nm node SRAM sample"

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