APPLICATION NOTE

Defect Localization at Transistor Gate using Electron Beam Induced Resistance Change (EBIRCh)

In collaboration with:

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Point Electronic GmbH
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INTRODUCTION

In the field of semiconductor Electrical Failure Analysis (EFA), many techniques use the electron beam of a Scanning Electron Microscope (SEM) for defect localization. These techniques use different types of beam/sample interactions to highlight defects: from the current induced by the electron beam into the sample, to the accumulation of charges on the sample or even the reaction of the sample to incoming electrons. The choice of the technique depends on the physical nature of the defect.

Among the most popular techniques, Resistance Contrast Imaging (RCI) and Electron Beam Induced Current (EBIC) are current collection techniques requiring the electrical contact of two probes with the sample. The electron beam scans over the sample while one of the probes amplifies the current that has been either induced in the sample by the electron beam (EBIC), or directly absorbed from the electron beam (RCI). The other probe is usually connected to ground. This provides another escape route for the charges than the signal probe, which increases contrast on the image. This allows to map resistance in the case of RCI and map electric fields in the case of EBIC. These techniques have been widely used to localize resistive defects, such as shorts between metal lines, or defects acting like charges generation/recombination sites, such as crystalline dislocations [1][2][3].

The newcomer to the family of EFA techniques is EBIRCh (Electron Beam Induced Resistance Change) [4]. Like EBIC and RCI, it is a specimen current technique requiring the use of two probes and a current amplifier. However, instead of mapping resistance like RCI, it is used to map resistance behavior of the sample, i.e. how the resistance of the sample changes over electron beam exposure (Figure 1). EBIRCh is therefore analogous to Optical Beam Induced Resistance Change (OBIRCh). It uses the electron beam instead of the laser beam to induce the resistance change, which makes EBIRCh not limited by the resolution of light and therefore allows much better defect localization. To measure resistance changes, a bias is applied between the two probes and the current flowing between them is monitored while the electron beam is scanned on the sample. Whenever the electron beam induces a resistance change in the sample, the current flowing between the two probes will change accordingly and generate contrast on the EBIRCh image. Hence, this technique can be used to locate all types of defects sensitive

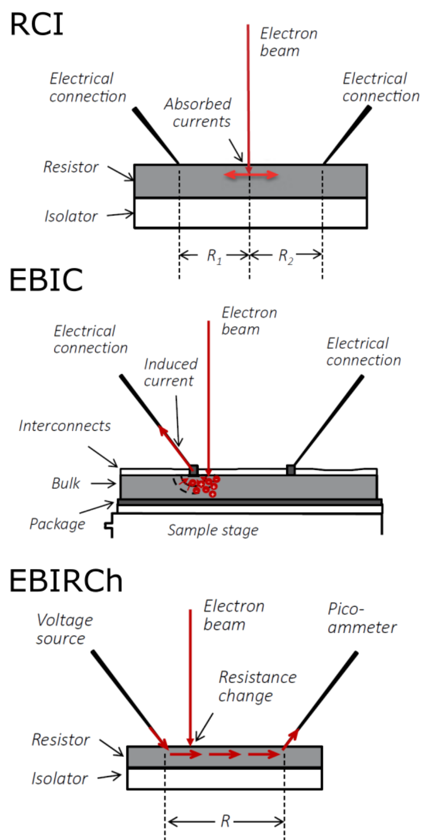

Figure 1. Schematics of interactions between the electron beam and the sample for three EFA techniques. The charges from the electron beam are either directly absorbed (RCI), or they generate secondary charges (EBIC), or they make the resistance of the sample change (EBIRCh).

to the electron beam. But EBIRCh is at its best at localizing high resistive defects in oxides, which is difficult to do with other techniques. In this note, we report about an experiment where EBIRCh was used to localize a defect within the gate oxide of a transistor.

EXPERIMENTAL SETUP

The FA engineers of Dialog Semiconductor PLC needed to find the leakage path at a defective transistor from a 130nm technology node sample. The sample was delayered to contacts level and mounted at the center of a *Nanoprobing Platform (SM100)* equipped with an *Active Sample Holder (ASH19)* and two miBot™ nanoprobers (Imina Technologies SA). 100nm Tungsten probes were loaded on the miBot™. The platform was mounted at the beginning of the experiment on the motorized stage of a *Helios NanoLab™ G3 CX DualBeam™* FIB/SEM (Thermo Fisher Scientific Inc.) (Figure 2) and removed at the end. The two probes were connected to an electrical failure analysis solution (Point Electronic GmbH). All electrical connections with the nanoprobing platform were made through the feedthrough connectors of the flange delivered with the system.

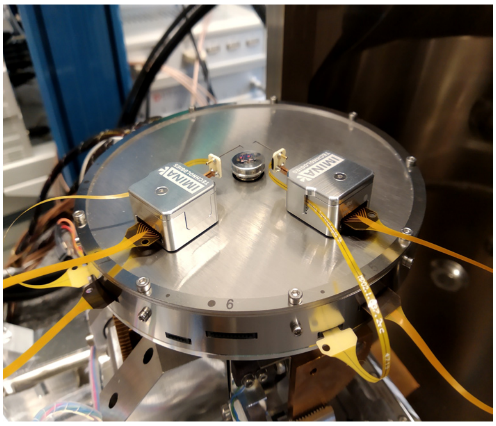

Figure 2. Two Imina Technologies miBot™ nanoprobers near the semiconductor sample to test. The Nanoprobing Platform is mounted on the SEM motorized stage.

METHOD AND RESULTS

To perform an EBIRCh measurement, it is necessary to determine the bias that will be applied between the two probes. It is usually done by acquiring an I/V curve between the two terminals of interests and selecting a voltage/current pair (working point) on this curve (Figure 3). To record it, the two probes were landed on the gate and bulk of the defective transistor. As several minutes may be required to execute the following steps, the stability of the probes must be high to maintain a reliable electrical contact with the transistor terminals during that time. The I/V curve measured between these terminals highlights the existence of a leakage current of several nA through the gate oxide of the transistor (Figure 3), confirming the existence of a defect. From this curve, a voltage/current pair of 0.3V and 300pA was chosen as the base working point for EBIRCh acquisition. Such a small current is a tradeoff between minimizing heating effects, and therefore the risk of modifying the defect, while still being high enough to be detected by the high-sensitivity current amplifier of the electrical analysis system. This bias was applied to the ground probe (Figure 4.1), while a reverse current of the same amplitude was applied through the electronics to the input of the current amplifier (Figure 4.2). The sum of these two currents leads to a zero current at the input of the amplifier. Therefore, only a change of current resulting from a resistance change induced by the e-beam (Figure 4.3) will be amplified by the current amplifier (Figure 4.4). The resistance behavior of the sample is then mapped into an image, displaying resistance changes as bright spots over a dark background.

To reach the defect in the gate oxide with the electron beam, it was experimentally determined that an acceleration voltage of 10kV was necessary. Higher or lower acceleration voltage lead to weaker resistance change signals.

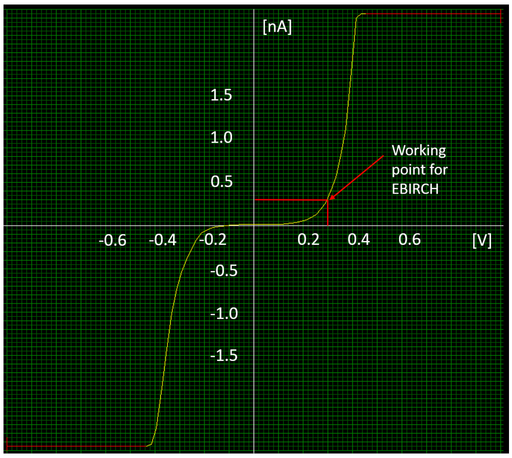

Figure 3. I/V curve recorded between gate and bulk of the defective transistor. Current has been limited to 2.5nA to avoid further damages at the gate oxide.

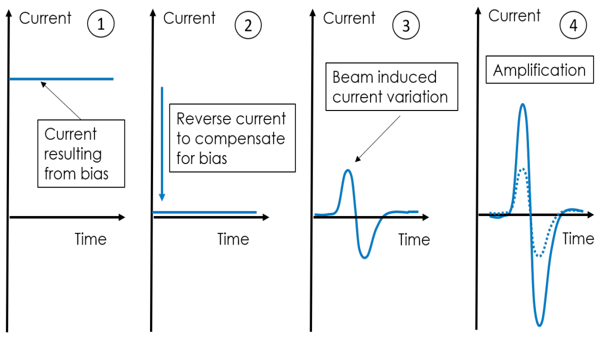

Figure 4. Working principle of EBIRCh detection. 1) A voltage bias is applied to the sample. 2) A reversed current is sent to the amplifier to compensate for the bias. 3) and 4) Any beam induced resistance variation is amplified.

The beam current was set to 86pA while the amplifier and imaging parameters were adjusted to maximize the signal without saturating the amplifier. An overlay of the SEM image (grayscale) together with the EBIRCh image (red levels) is presented on Figure 5.

On this image, a bright red spot of 59nm can be identified. It is the location in the sample where the resistance between the two probes changes the most upon electron beam exposure. It corresponds to the location of the defect in the gate oxide, and its position is known within tens of nanometers. The high accuracy of the defect localization obtained in this case allows the failure analyst to be certain that the defect will be contained in a single TEM lamella prepared from the vicinity of the spot, avoiding the preparation and observation of several TEM lamellas not containing the defect.

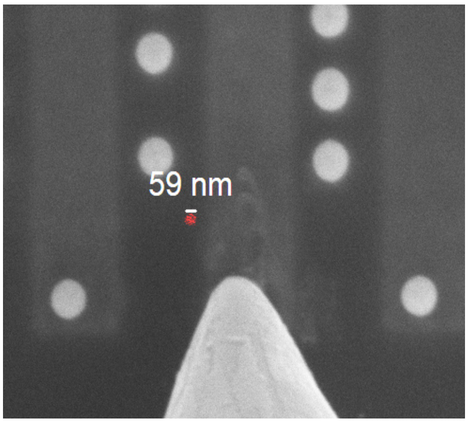

Figure 5. Overlay of Secondary Electron image and EBIRCh image. A spot of 59nm is highlighting the location of the defect in the gate oxide.

CONCLUSION

In this note, we describe the use of the EBIRCh technique to accurately locate a defect in the gate oxide of one of the transistors of a semiconductor device. The success of this experiment was made possible thanks to the high positioning accuracy and stability of the nanoprobing system of Imina Technologies SA, as well as the low noise and high sensitivity of the current amplifier of the electrical measurement system of Point Electronic GmbH. With these, it was possible to use the SEM at low beam current and low probe voltage which reduced the risks of modification of the defect while allowing its localization in only a few tens of nanometers.

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[3] C. Ramachandra, J. Venkatesh, Sarat Kumar Dash, " Passive Voltage Contrast Technique for Semiconductor Device Analysis", International Journal of Engineering and Advanced Technology, 2017.
[4] Gregory M. Johnson, "Electron Beam Induced Resistance Change for Device Characterization and Defect Localization", International Symposium for Testing and Failure Analysis, 2016.

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