APPLICATION NOTE

Nanoprobing SEM Solution for In Situ Semiconductor Failure Analysis

Failure analysis measurements for automotive industry are conducted to identify and localize fabrication defects in transistors and integrated circuits interconnections. Resistivity measurements, transistor characterization, EBIC and EBAC are here performed with Imina Technologies nanoprobing platform and successfully used to achieve this goal.

In collaboration with:
Fraunhofer CAM
Halle, Germany
www.cam.fraunhofer.de

Imina Technologies products in use:
- miBot™ BT-14 nanomanipulator
- Nanoprobing SEM Platform kit

INTRODUCTION

The number of microelectronic devices integrated in modern cars has dramatically increased in the past years, yet the reliability has to remain excellent. This is a major challenge for the automotive industry. Semiconductor failure analysis methods have therefore to continuously improve in order to withstand it. In fact, conventional failure analyses techniques such as emission microscopy (EMMI) and optical-beam-induced resistance change (OBIRCH) alone are no more sufficient to localize and identify defective structures. Additional electrical characterization of single IC structures is required. Nanoprobing, Electron Beam Induced Current (EBIC) and Electron Beam Absorbed Current (EBAC) are advanced characterization methods developed for that purpose. They enable the failure investigator to gain insights into the failing component on the chip after rough localization using the conventional techniques. Due to the limited number of available defective components—typically one—on which investigators have to carry out their analysis, the success rate must be as close as possible to 100%.

This application note presents a case study of nanoprobing investigations conducted at the Fraunhofer CAM (Halle, Germany) using Imina Technologies miBot™ nanomanipulators to detect and localized defects on automotive electronic devices.

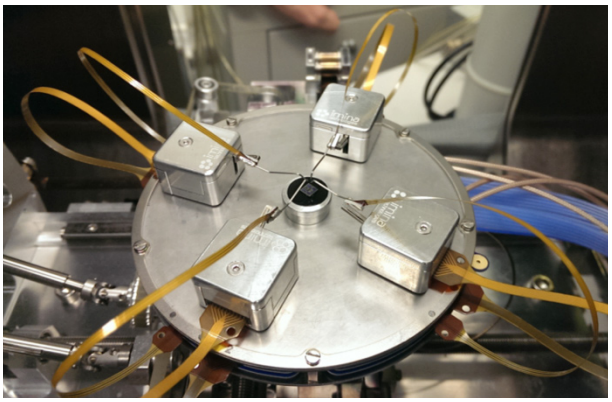

Figure 1. Four miBot™ nanomanipulators placed around the device under test on a Nanoprobing SEM Platform. The platform is mounted on the SEM sample stage.

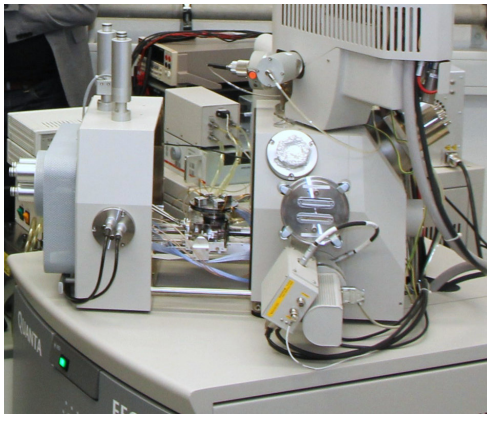

Figure 2. Photograph of the FEI Quanta 650 ESEM that was used for the experiments.

EXPERIMENTAL SETUP

The measurements presented hereafter were performed with the Imina Technologies Nanoprobing SEM solution loaded with four miBots and the device under test [Figure 1]. The platform was installed in a FEI Quanta 650 ESEM [Figure 2]. Electrical measurements were performed with a Keithley 4200-SCS semiconductor parametric analyzer. EBIC and EBAC analyses were made with a DISS 5 (Point Electronic GmbH).

MEASURES

Low resistivity measurements of VIA chains

An investigation of defects in metal networks generally leads to evidence of shorts or opens on metal lines and interconnections. However, in some cases, failing connections only cause an increase of resistivity. In this case, fine resistivity measurement between the two parts of the network under investigation is required.

Low resistivity measurements have been realized on a faulty VIA chains process monitoring structure [Figure 3]. The probing has been carried out at exposed alumina parts. Results are presented in Figure 4. The resistivity of the failing VIA chain shows a value of 225 Ω and is 40% higher than the reference value of 160 Ω. A FIB cross section revealed a misalignment between a metal line and the relative interconnection, resulting in a reduced contact surface.

Transistors characterization

Transistor node sizes have kept decreasing down to a few tenths of a nanometer. This makes the characterization of a single transistor very challenging to carry out under a conventional probe station. To cope with probers lack of precision, metal pads are usually deposited around failing transistors with a FIB. This is a lengthy process which also comes with an intrinsic drawback: a poor signal to noise ratio.

Nanoprobing overcomes both of these issues. In fact, the nanometer positioning resolution of a miBot™ manipulator enables the investigator to precisely put down probes directly on metal lines, significantly accelerating the process throughput.

In this example, PMOS transistor characteristics were measured with the nanoprobing method. First metallization levels were removed by chemical-mechanical polishing in order to isolate a single transistor and to have access to alumina metal lines. Then, four tungsten needles were put in contact with the source, drain, gate and well nodes of the transistor [Figure 5]. A Keithley 4200 SCS semiconductor characterization system was used to generate I/V curves of source and drain for several gate potentials [Figure 6].

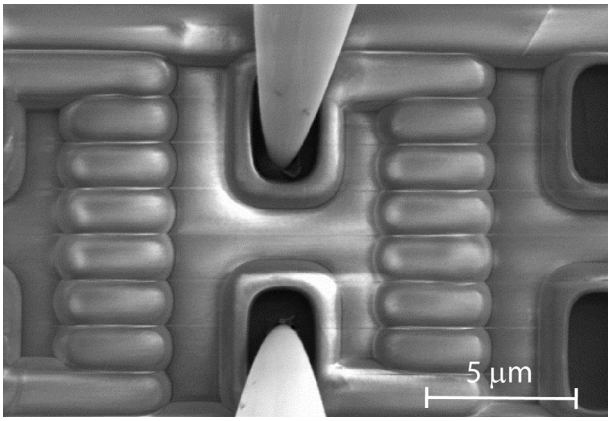

Figure 3. Probing at exposed alumina parts to investigate low ohmic VIA chains.

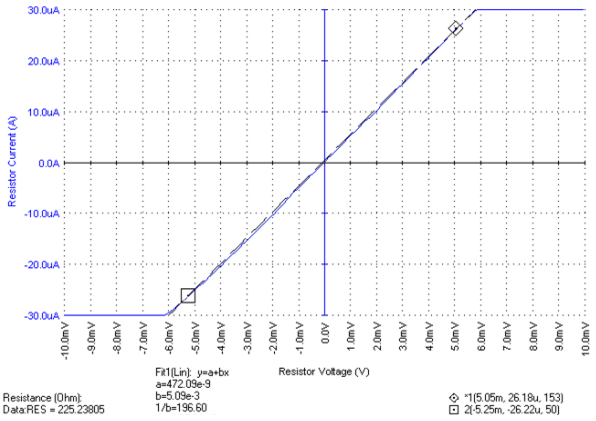

Figure 4. Resistivity measurement of VIA chains.

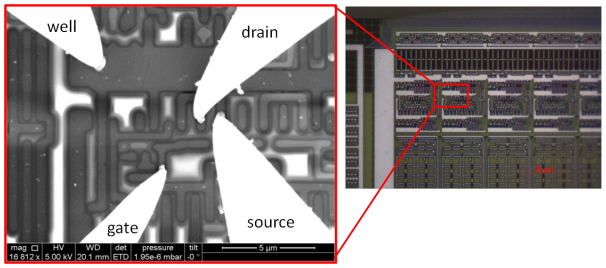

Figure 5. Electrical probing of a single PMOS transistor.

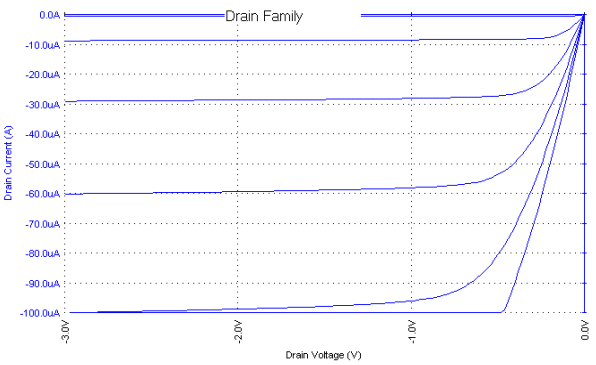

Figure 6. Transistor characteristics: I/V curves function of different gate voltage potentials.

SEM-BASED

Electron beam -induced current (EBIC) and -absorbed current (EBAC) are two techniques for accurate single component investigation. They take advantage of the interaction of the SEM electron beam with the device under test to reveal information to the failure analysis investigator. Both require a prior rough localization of the defect by means of other techniques such as OBIRCH, EMMI or lock in thermography (LiT).

EBIC for p-n junction investigations

Electrical transistor characterization has found differences between neighbor transistors. In particular a transistor has shown a reduced drain current in comparison to the reference one. EBIC is here used to shed light on this anomaly and understand the causes of this behavior. Indeed, high resolution EBIC provides the means to visualize and quantitatively determine properties like the position and diffusion length of transistor p-n junctions. The SEM electron beam induces electron-hole pairs which are separated by the internal electric field at the transistor p-n junction, creating an induced current.

Probe needles are placed in contact with the transistor source and well which are separated by a p-n junction. The electron beam generated current is mapped by the EBIC scanning system and overlaid to the microscope secondary electron image. The electron beam is incident on the PMOS transistor cross section with an acceleration voltage of 2 keV [Figure 7]. The cross section analysis allows a reduced electron accelerating voltage and therefore a very high resolution due to a small interaction volume.

The source depletion regions of the reference transistor and of the defective transistor are compared [Figure 8]. Investigators have seen that the defective transistor has a small overlap with the gate oxide structure in comparison to the reference transistor. This anomaly leads to a longer channel region of the defective transistor which causes the drain current reduction. The fabrication defect is therefore indentified with the short extension of the source p-n junction below the gate oxide.

EBAC for defect localization in metallization networks

The combination of resistivity measurements, presented above, and the EBAC technique provides a powerful means to characterize metal interconnects of integrated circuits. The EBAC technique is based on a similar principle as EBIC. The electron beam of the SEM scans the sample and injects charges inside a certain interaction volume. Injected charges are absorbed by metal lines under the surface. A current is then induced and measured by a probe placed at contact level on one end of the metal line of interest [Figure 9]. As for EBIC, the probed signal is overlaid on the secondary electron image. Direct comparison of this image with layout details allows the investigator to easily detect and finely localize shorts and/or opens.

Here, silicon is completely removed from the backside to access small lower metal lines. One miBot™ was used to probe at contact level (tungsten plugs with diameter of approximately 350 nm) to investigate metallization of a complete integrated circuit. The red color indicate that the metal lines are electrically connected to the manipulator probe [Figure 10].

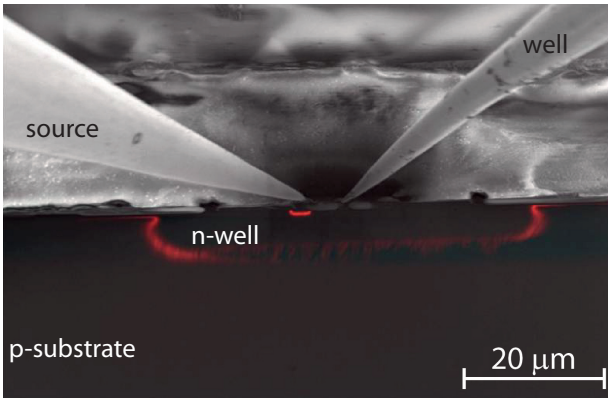

Figure 7. Large EBIC imaging of a double PMOS transistor cross section. The two probes are connecting respectively the right transistor source and the well. The red color represents the intensity of the EBIC induced current generated along the p-n junction depletion regions.

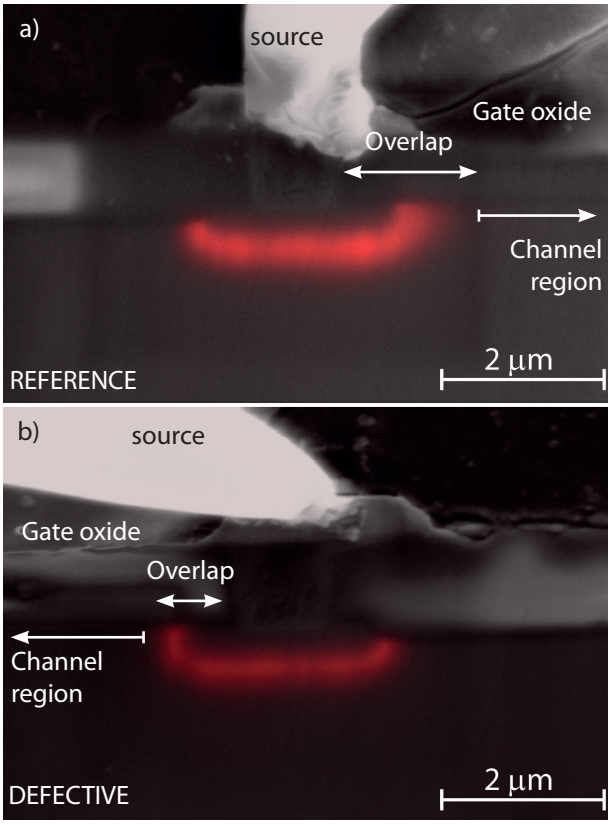

Figure 8. a) EBIC scan of the reference transistor source. The depletion region is extended along the channel region. b) EBIC scan of the defective transistor source. The depletion region is not enough extended along the channel region. This leads to a longer conductive channel and therefore to a higher transistor resistance.

CONCLUSIONS

Advanced failure analysis methods are required to develop reliable and fail-safe electronic devices for cars. They enable engineers to identify and understand failure mechanisms. Here, complementary techniques, such as transistor characterization and EBIC, are used to detect transistors behavior anomalies and to obtain information about the defects nature and their location. In addition, resistivity measurements and EBAC allow a precise localization of defects in metal interconnections.

This application note reports on how Imina Technologies' miBot™ nanomanipulators are key components to perform these failure analysis methods. Their nanometer resolution over several centimeters range of displacement provides precise positioning and safe landing of probe needles on the analyzed devices

Moreover, the miBot™ rotation around the vertical axis allows the user to adjust the probe's orientation in situ without need to open the SEM chamber, resulting in higher throughput experiments.

Finally, the compactness of the miBot™ contributes in drastically reducing both the mechanical and thermal drifts compared to other marketed nanopositioning technologies. This unmatched stability ensures reliable and steady measurements over long period of time.

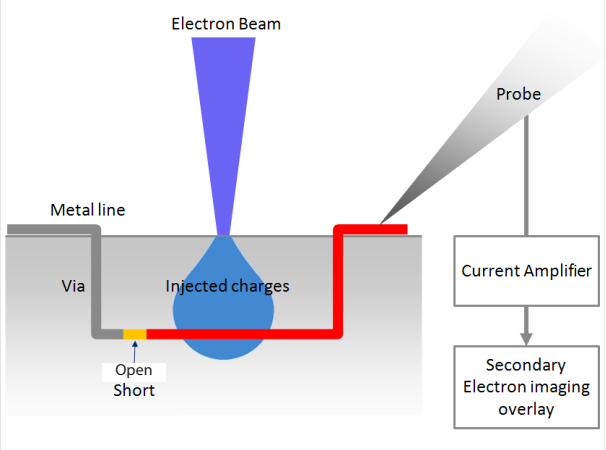

Figure 9. Schematic of the EBAC characterization principle.

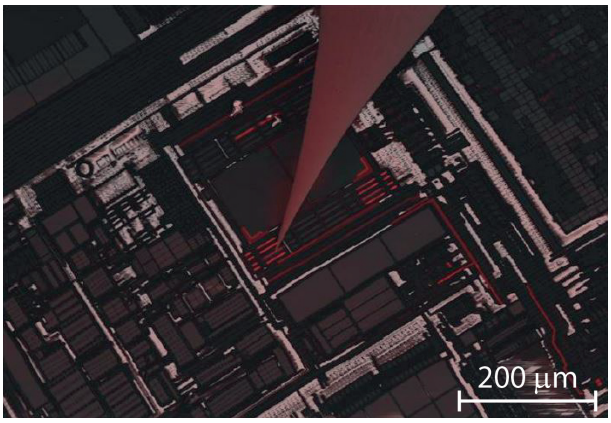

Figure 10. Backside of an integrated circuits analyzed with EBAC technique. In red, the absorbed current flowing in the metal lines linked with the probe. The electron beam accelerating voltage for EBAC measurements is 10 keV.

ACKNOWLEDGEMENTS

This application has benefited from the expertise in semiconductor failure analysis from Frank Altmann's team at Fraunhofer CAM. We would like to thank Frank Altmann, Jörg Jatzkowski, Michél Simon-Najasek and Christian Grosse for their help.

Imina Technologies SA
Route de Montheron 8b, 1053 Cugy (VD), Switzerland
www.imina.ch