IMINA
TECHNOLOGIES

APPLICATION NOTE

Threefold speed-up in the characterization of 7 nm SRAM transistors using an XYZ sample substage

INTRODUCTION

Depending on transistors' size and location on the chip, electrical characterization can be a time-consuming and complicated task. For the smallest technology nodes hidden deep in the stack of a semiconductor chip, electrical nanoprobing is the final step to characterize the electrical properties of transistors. Before such measurements can be done, multiple-step sample preparation is required to open the stack (mechanical or chemical polishing, focus-ion-beam processing, etc). Once the sample is ready for nanoprobing, it is still a complicated and time-consuming procedure.

When probing the nodes smaller than 45 nm with high-κ materials in the gate stack, one has to operate SEM under low acceleration voltage and short working distance. These imaging conditions result in comparatively poor image contrast, making it challenging for the operator to navigate around the sample and to contact the device under test (DUT).

To study the homogeneity of electrical properties across the sample or to find the area with specific conditions, several devices need to be tested in different locations. Here, we show how an XYZ sample substage helps to reduce the time it takes to bring the probes to different locations. It brings the regions of interest (ROI) to the probes instead of moving each probe individually, so just the final touch to electrical contact needs to be made by the operator. We characterize 7 nm technology node SRAM chip on M1 level as an example, and find the area that is not covered by residual oxide after delayering.

EXPERIMENTAL SETUP

The following electrical probing setup is used and installed in a Zeiss Gemini 300 SEM:

• Imina Technologies' nanoprobing platform equipped with Sample Positioning XYZ Sub-Stage with four miBots™

• Tungsten probes with tip curvature radius of 10 nm, the tip bent at 40° for each miBot™.

• Semiconductor parameter analyzer (Keithley 4200A-SCS) equipped with four 4210-SMU modules operated from Imina Technologies Precisio™ software.
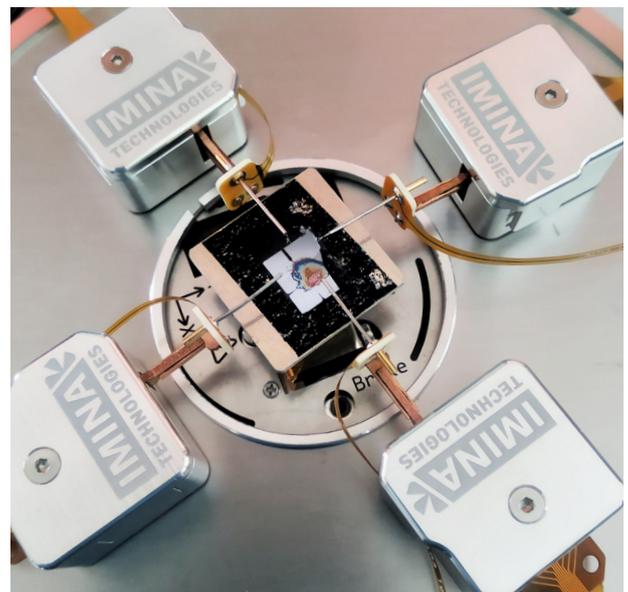

Figure 1. Four miBot™ nanoprobers around a semiconductor sample to test. The platform is mounted on the SEM motorized stage.
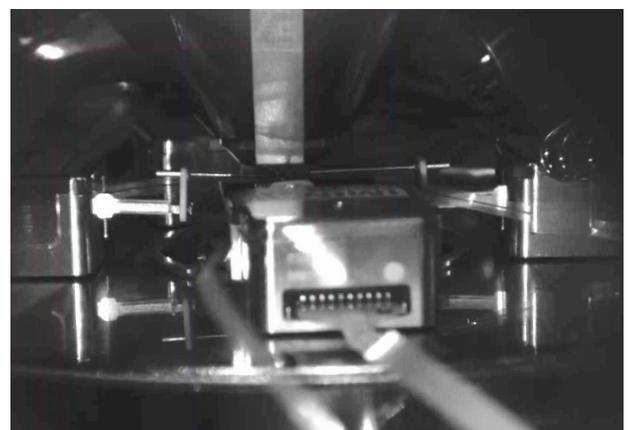

Figure 2. View from the SEM chamber scope on the miBot™ nanoprobers above the sample with a 2.8 mm working distance.

MEASUREMENTS PARAMETERS

Notations

I_D – Drain current

V_{DS} – Drain-Source voltage

V_{GS} – Gate-Source voltage

I_S – Source current

Sequence to measure the ID and IS

• VG steps of 0.5V.

• NMOS: Sweep VD (ID=f(VD)) in 0.025 V steps at different values of VG.

All the measurements are run directly from Imina Technologies' Precisio™ software. The results are displayed immediately on a plot and as a table of values. All data are stored in Precisio™ database along with the parameters of the test recipe for post-processing and reporting.

Figure 3. Configuration of electrical test recipes in Precisio™ software for the remotely controlled semiconductor parameter analyzer

SAMPLE PREPARATION AND CHARACTERIZATION

The sample used here is a large SRAM region. Mechanical delayering resulted in a non-uniform material removal and exposed different layers at different regions, with layers transition between these regions. We suspect that this sample preparation will render only part of the delayered area suitable for measurements and use electrical nanoprobing across the sample to identify locations that were properly delayered.

The sample was placed on the electrically active stub holder that can be grounded or biased, at the center of the nanoprobing platform on an XYZ substage. After a short in-situ plasma cleaning, the acceleration voltage of the SEM was set at 500 V at 2.8 mm working distance.

To find a first candidate for transistor characterization, the probes were rapidly lowered one by one. The sample was then raised towards the probes using the Z axis of the substage until its features were nearly at the same focus as the probes. Finally, the sample was laterally moved under the probes to find a suitable device. When the right spot was found, the probe tips were sequentially lowered using manual controls until they were in good electrical contact with each transistor node.

Although M1 contacts could be identified at the first ROI, the electrical measurements on these transistors did not give satisfactory results. Figure 3 shows the probes landed on an NMOS transistor and the corresponding curves. The probes couldn't establish good contact with the sample, with the resulting curves being mostly resistive with very low current. The most likely reason for such results would be a thin oxide layer remaining on the contacts at this specific location. The contacts would be still visible because the penetration depth of the electron beam can render the features that are slightly below the surface, even if these features are not exposed. But the electrical contact to the devices in this ROI would not be possible.

To navigate to the second ROI, the sample was first lowered and retracted from the probes to prevent any probe damage. This movement was possible thanks to the gentle DC movement of the Z stage. Then, the sample was moved in XY below the probes until the second ROI was identified.
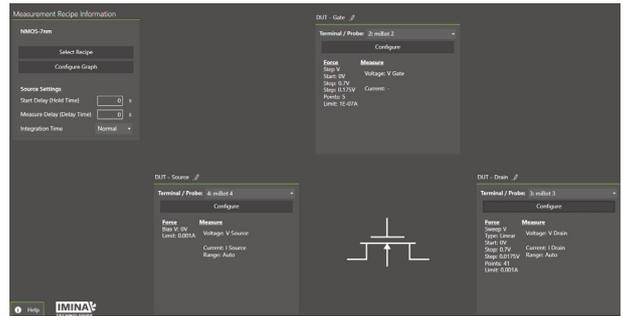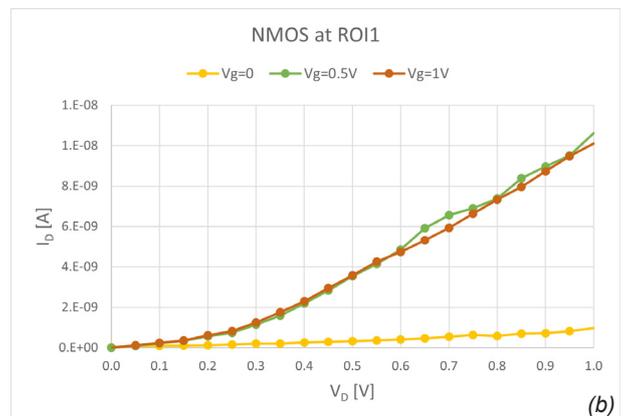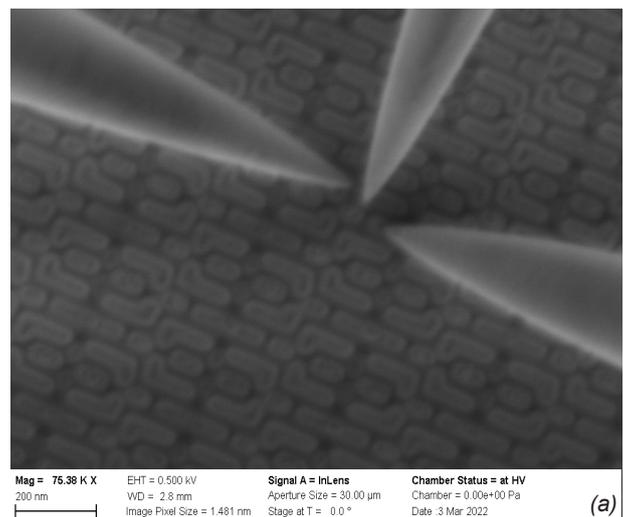

Figure 4 .
(a) SEM image of the 3 probes landed on a NMOS transistor at ROI1.
(b) Corresponding Vd-Id curves recorded on this transistor showed no electrical contact.

The sample was lifted back to the probes to bring a NMOS in contact with the probes. During the whole process, the probes had to move less than 100 nm to finely adjust their position on the transistor. The remaining movements were all done using the sample XYZ substage, greatly speeding up the procedure.

The measurements were repeated on this NMOS transistor and are shown in Figure 4. At this ROI, the edges and contrast of the contacts were sharper, indicating less or none of the remaining oxide layer. The measurements confirmed the latter suggestion, as the IV curves show typical NMOS behavior.

DISCUSSION

Sample XYZ substage helped to reduce the characterization time threefold as compared to the measurements without the substage. The time needed to move the sample from one ROI to the next using the XYZ substage is approximately the same as the time it takes to move one probe between ROIs. With three probes used in this experiment, we need three times more time to change ROI if the XYZ sample substage is not available.

Consistent and smooth curves measured in the second ROI confirm that the contacts in the first ROI were not exposed.

The normalized standard deviation of difference between Drain and Source current is smaller than 1% over the measured range. Such low value highlights the excellent stability of the contact resistance during measurement. Noise and measurement resolution: on NMOS transistor at VGS = 0V (transistor OFF), Drain current ID < 10 pA at VDS = 0V and ID < 2 nA at VDS = 0.7V.

Mag = 124.16 K X | EHT = 0.500 kV | Signal A = InLens | Chamber Status = at HV
100 nm | WD = 2.8 mm | Aperture Size = 30.00 μm | Chamber = 0.00e+00 Pa
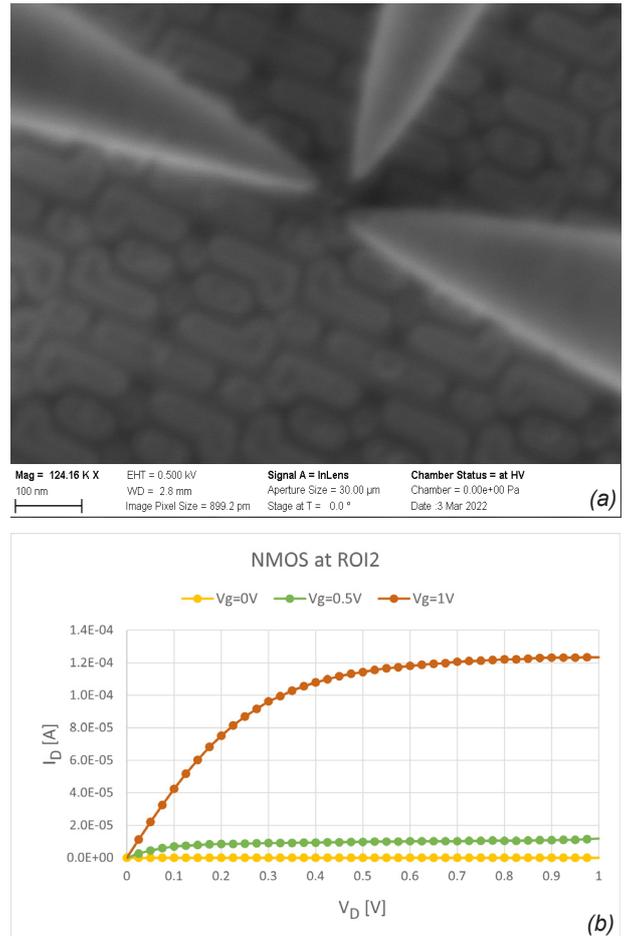| Image Pixel Size = 899.2 pm | Stage at T = 0.0 ° | Date :3 Mar 2022 | *(a)*

Figure 5.
(a) SEM image of the 3 probes landed on a NMOS transistor at ROI2.
(b) Corresponding Vd-Id curves recorded on this transistor.

CONCLUSIONS

Some challenges such as imaging conditions can't be avoided, but other aspects of the nanoprobing workflow can be optimized. We have conducted nanoprobing experiments to characterize different NMOS transistors of a 7 nm semiconductor technology nodes using Imina Technologies' XYZ sample substage. The results highlight the capability of Imina Technologies' Nanoprobing Solutions to perform reliable measurements on such small nodes. The Sample Positioning XYZ Sub-Stage helps to optimize the workflow by enabling fast lateral movement from one ROI to another, without having to move the probers one by one. It also helps to quickly approach the sample to the probes or to retract it from them. As a result, the 7 nm transistor characterization was three times faster than without the Sub-Stage.

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The system's shielded cabling enables transistor characterizations with excellent signal-to-noise ratio. The operator is assisted at each step of the nanoprobing workflow: the nanoprobers placement around the device under test, landing the probe tips in contact, setting up test recipes, running measurements and storing data.

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