APPLICATION NOTE

Failure mechanisms of single bits in a flash memory array

INTRODUCTION

There are two ways to increase the bit density on a chip without increasing dimensions: reduce average bit size, or to stack more bits on top of each other to increase their volume on the same chip area (vertical NAND-chips, 3D-IC design, chips stacking, …). Both approaches result in higher device complexity, and make it harder to find failures.

Flash memory is a type of electrically erasable programmable read-only memory (EEPROM), which is now replacing hard drive technology in most applications. Each bit can be addressed at the end of production for a functional test. This way, it is possible to identify the failing bits.

Functional tests can only read 0 or 1 values stored in a bit so they cannot yield information about the origin of the problem. To know what happened to a malfunctioning bit, we need to determine which transistor is responsible for the issue, and to find out more about the failure mechanism (see Fig. 1 for the bit structure).

In this application note, we will compare the Write, Erase and Read cycles of working and faulty bits at the contact level. The main challenge of such measurement is that it requires landing probes on 5 different terminals and maintaining a good electrical contact during the whole measurement. We will also investigate how the bit behavior is influenced by long exposure to the e-beam.

DEVICE UNDER TEST

A sample of a flash EEPROM with multiple failing bits identified in a functional test, delayered to expose 100nm contacts. The structure of the memory array is as follow:

The Word Line of the memory array is connected to the Control Gate of an NMOS transistor. This gate gives access to several bits, each consisting of a floating gate and a Drain contact (Bit Lines). A Source contact is common for all bits. A contact to the gate of the Select transistor is also available to select a group of bits. An individual bit cell can be modelled as shown in Fig. 2.

EXPERIMENTAL SETUP

The following electrical probing setup is used in a Zeiss Sigma SEM:

- Imina Technologies' nanoprobing platform equipped with five miBots™
- Semiconductor parameter analyzer (Keithley 4200A-SCS) operated from Imina Technologies Precisio™ software (Nanoprobing Workflow edition 2022).

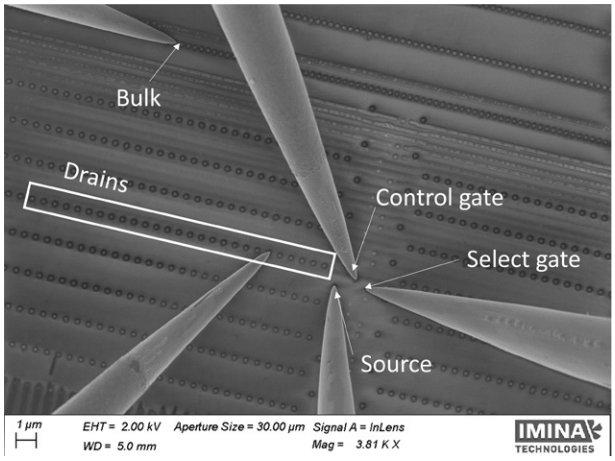


Figure 1. Structure of a Flash EERPOM memory array, with nanoprobes landed on five terminals.

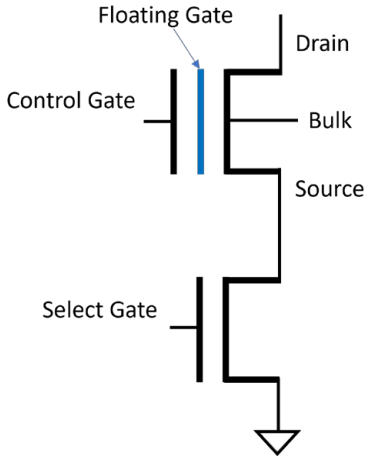


Figure 2. Schematic of a Flash EEPROM memory bit.

During its life cycle, such a bit cell is submitted to different bit operations such as Write, Erase, Read and Disturb. Indications on the voltage values applied to its terminals during these operations are presented in the table on the right*.

But to understand the possible failure mechanisms for a bit, it is necessary to understand the charge transport in the bit cell during each of these operations as well as the effect of such charges on the transistor properties.

Write: large positive voltage (V_{WR}>>0) on the control gate moves electrons from the drain to the floating gate. As the floating gate becomes negatively charged, a higher Control Gate voltage (V_{CG}) is necessary to make the transistor channel conductive.

Erase: large negative voltage (V_{ER}<<0) on the control gate removes electrons from the floating gate towards the bulk. The floating gate becomes positively charged, so a lower V_{CG} is sufficient to make the transistor channel conductive

Read: a sweep on V_{CG} determines the threshold voltage (V_{th}) of the transistor. The value of V_{th} tells us if the control gate is charged positively (low V_{th}) or negatively (high V_{th}).

Disturb: By applying an intermediate positive voltage to the Control Gate (< V_{WR}) and a positive voltage to the Drain, we simulate what a bit sees when a bit close to it is being written or read. The voltage difference between Drain and Control Gate is usually not sufficient to tunnel electrons to the floating gate. Even though one of such event is not sufficient to write a previously erased bit, the large size of memory array means that a bit can be exposed thousands of times to the Disturb cycle before being read again.

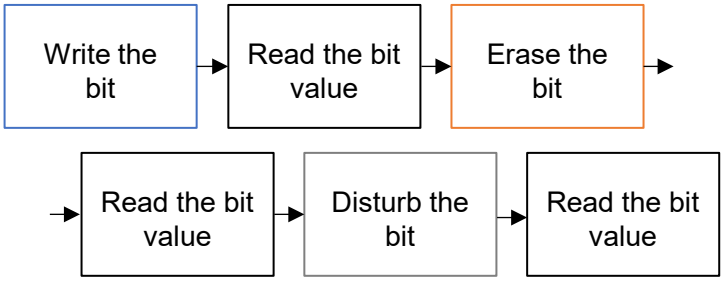
	Control Gate	Select Gate	Drain	Source	Bulk
Write	V_{WR}>>0	0	0	0	0
Erase	V_{ER}<<0	0	0	0	0
Disturb	0<V_{Dis_G}< V_{WR}	0	V_{Dis_D}>0	0	0
Read	Sweep	V_{SG}>0	VD>0	0	0

**Due to confidentiality we're not allowed to show the voltage values*

UNDERSTANDING THE FAILURE MECHANISM OF THE FAULTY BIT

To perform the basic operations of a memory cell and to characterize the Control transistor, we land the probes on all five terminals of a bit. Before troubleshooting the faulty bit, we characterize a functioning one to get a reference.

Once the probes are in contact with the Control and Select Gates, Drain, Source and Bulk of the functioning bit, the following sequence is performed:



The same sequence was repeated on a bit known to be not working properly.

In Fig. 3 (top), we see that after the Write cycle, the control gate voltage needed to close the transistor is much higher than the one needed at the Erased state. A disturb cycle barely shifts the characteristics from the Erased state, the bit stays Erased.

The functional and the faulty bit behave similarly after Write and Erase cycles, see Fig. 3 (bottom). The Disturb cycle shifts the characteristics of the faulty bit towards the Write state. As

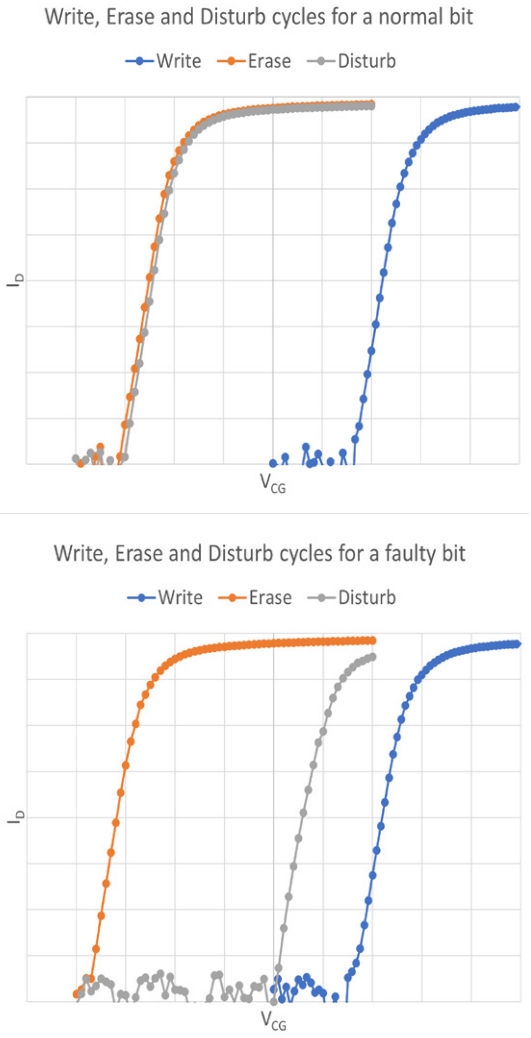


Figure 3. Drain current (log scale) as a function of Control Gate voltage during Write, Erase and Disturb cycles for a normal (top) and a faulty bit (bottom). Range of values on both plots is the same (values cannot be shown due to confidentiality).

a result, the bit changes its value when it is not supposed to. This is why the bit was identified as faulty in the functional tests: the voltage repeatedly “seen” by the Control Gate of this bit while other bits were written was enough to partially write it.

To better understand how the faulty bit fails, we characterize its Control transistor. We found that the leakage between the Drain and Bulk of the Control transistor is a few orders of magnitude larger than that in the functioning bit’s Control transistor (which is negligible), as shown in Fig. 4. This finding suggests that the failure is caused by a defect between the Drain and Bulk of this transistor, which can be further investigated by FIB-TEM.

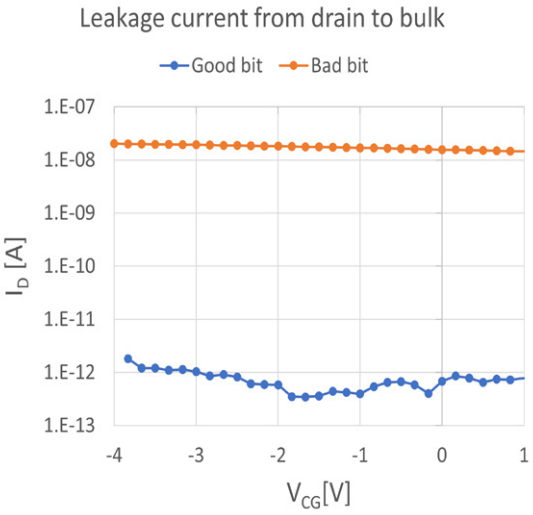


Figure 4. Comparison of Drain-to-Bulk leakage current in the functional (blue) and faulty (orange) bit.

INFLUENCE OF THE ELECTRON BEAM ON THE BIT VALUE

To study if bit integrity is influenced by exposure to the electron beam from the SEM, we read the functional bit’s value before and after exposure to the e-beam.

Using an acceleration voltage of 2kV, we imaged the drain of the bit for a few minutes. The probing needles were not in contact with the sample. After the exposure, we landed the needles again and read the bit. We found that the bit with value ‘1’ changed value to ‘0’, as shown in Fig. 5 -- it was effectively erased by the beam. This means that the Floating Gate got positively charged due to the exposure. The exact mechanism of how it happened needs further investigation.

This finding stresses the need for low kV imaging and proper grounding of the control gate while imaging.

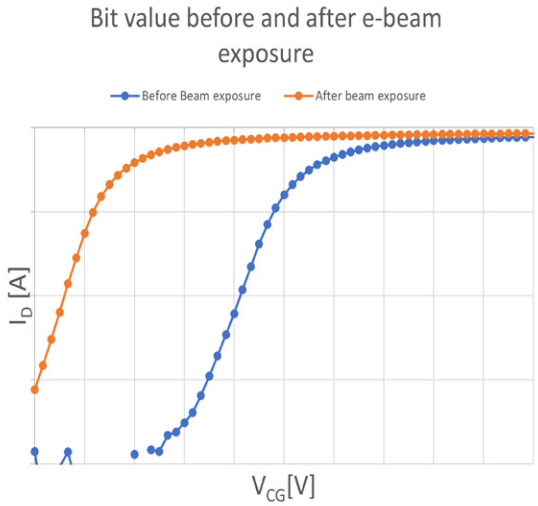


Figure 5. Drain current (log scale) as a function of Control Gate voltage during Read cycles for a functional bit before (blue) and after (orange) exposure to e-beam. Values are not shown due to confidentiality.

CONCLUSIONS

We compared behavior of functional and faulty bits in a flash memory array. We found that the faulty bit changed its value after being disturbed by operations on other bits around it. Further measurements showed that in the faulty bit, the leakage current between the Drain and the Bulk was several orders of magnitude higher than that in the functional one. This leakage suggests that there is an unwanted resistive behavior between Drain and Bulk, which can be further located by electron beam analysis techniques (EBIC/EBAC/EBIRCH) and investigated by FIB-TEM.

We have also studied the effect of e-beam on functional bits. After a few minutes’ exposure to the 2keV electron beam, the bit value was erased. We conclude that relatively high energy electrons have the same effect on the bit as a strong negative voltage applied to the Control Gate.

Nanoprobing is a powerful tool to investigate failure mechanisms in flash memory arrays. Successful investigation requires to land five probes and maintain them in good contact, while keeping e-beam exposure to the minimum. Imina Technologies’ nanoprobing solution allows to perform this task efficiently thanks to the intuitive tip landing procedure and excellent probe stability with drift <1 nm/min.

Imina Technologies SA
Route de Montheron 8b, 1053 Cugy (VD), Switzerland
www.imina.ch