APPLICATION NOTE

Thermal behavior of a PMOS transistor

Semiconductor devices are typically designed to operate between 0 and 70 °C, which is considered the normal operating temperature range. Sometimes though, devices get to work at lower or higher temperatures. Away from the normal operating temperature range, devices may consume more power, leak current or crack due to the thermal expansion, and overall be less reliable in the long-term. Specific behavior of transistors at different temperatures can vary depending on the transistor technology, design, and the materials used. Testing thermal behavior of a given device is an important part of quality assurance and risk management.

Our thermal stage for in-situ SEM nanoprobing covers temperature range from -30 to 150 °C. This range corresponds to the practical extension of normal operation conditions for semiconductor devices or can be used for accelerated testing to predict the lifetime of a device in normal conditions from its behavior at 150 °C.

At high temperature, we expect a decrease in threshold voltage (the voltage at which the transistor starts conducting) and drain current at saturation (current that flows between the drain and source terminals when transistor is on) and an increase in off-current (current that flows between the drain and source terminals when transistor is off).

In this application note, we test thermal behavior of a PMOS transistor of 180 nm technology node. The transistor has been delayered to contact level and loaded into TESCAN Clara SEM equipped with Imina technologies' NANO system with a thermal stage. We analyze how threshold voltage, drain current at saturation and off-current behave at -30, 75 and 150 °C.

Figure 1 shows that at higher temperature, the drain current increases at lower gate voltage, which means that the threshold voltage decreases.

To test the off-current behavior, we apply no voltage to the gate to keep the transistor in its off state. In Figure 2, we observe that the drain current is higher at higher temperature, which is what we expected.

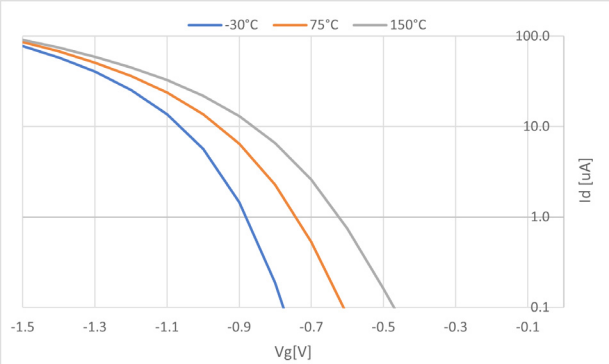

Figure 1. Investigating threshold voltage. A log plot of drain current ID as a function of gate voltage V_G.

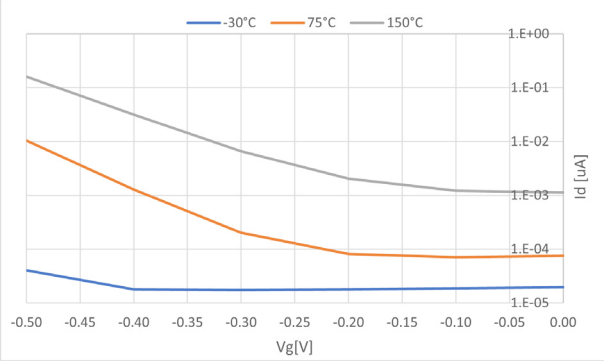

Figure 2. Testing the off-current. A log plot of drain current I_D as a function of gate voltage V_G. On this plot, the current values at V_G=0 correspond to the off-current, and a larger VG range is shown to highlight the trend at each temperature.

Figure 3 shows the IV curve for V_G from 0 to -3V. At V_G =-1V, the current is higher for high temperatures, which means lower V_{TH} for these temperatures. At the far left of the plot, the drain voltage and the gate voltage are at -3V. At these voltages, we reach I_{DSAT}, and therefore we conclude that I_{DSAT} decreases with temperature.

Conclusions

In this series of measurements, we have tested how a PMOS transistor changes its behavior at different temperatures. We observed the expected decrease in threshold voltage and current at saturation, and a decrease in off-current, which suggests higher leakage.

With our thermal stage, such measurements can be done in-situ SEM, and the users can leverage all benefits of miBot nanoprobers, such as freedom of movement around the platform, and easy and precise probe landing.

Thermal stage is an optional module for Imina Technologies' NANO 8-bot system. Existing setups can be upgraded with the thermal stage, as long as Precisio software is updated to the latest version that includes the thermal stage control module.

Contact us if you are interested in our thermal stage, or if you would like to incorporate thermal sample analysis in the nanoprobing service.

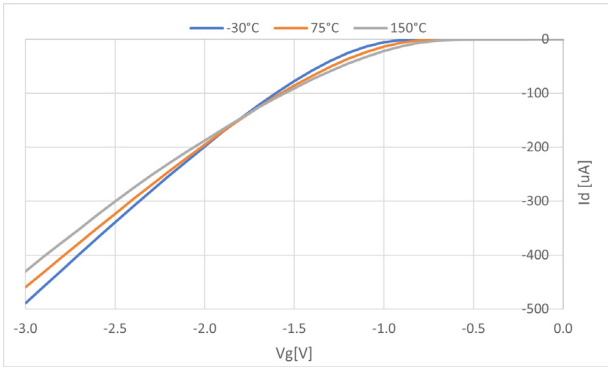

Figure 3. Investigating drain current at saturation. A plot of drain current I_D as a function of gate voltage V_G.

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